Network-on-Chip for a Partially Reconfigurable FPGA System

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ABSTRACT

A custom FPGA-based, 1U CubeSat form-factor reconfigurable computing development platform has been designed and built for the purpose of implementing and testing multicore and multiprocessor systems. The platform was designed to leverage the active partial reconfiguration and configuration readback capabilities of the Xilinx Virtex-6 device. This enables myriad research opportunities in parallel processing, high-performance reconfigurable computing, and multicore/multiprocessor system design. An example application features a nine-processor radiation tolerant computer system which motivates further research into network-on-chip solutions for reducing multicore system routing complexity.

Categories and Subject Descriptors

C.4 [**Performance of Systems**]: Fault tolerance;
J.2 [**Physical Sciences and Engineering**]: Aerospace

Keywords

Reconfigurable computing, FPGA, fault tolerant, network-on-chip, partial reconfiguration, readback

1. INTRODUCTION

The presented system is a highly flexible, FPGA-based, general-purpose reconfigurable computing platform designed to enable research in numerous areas related to computer architecture. Some of the research areas of interest include high-performance computing, parallel processing, reconfigurable computing, multicore and multiprocessor system design, fault-tolerant architecture design, and interconnect on multicore or multiprocessor systems. A current multiprocessor research system demonstrates the need for a network-on-chip (NoC) to alleviate the complexity of inter-tile routing. This system is a radiation tolerant reconfigurable computer designed and implemented on the research hardware. It features nine Microblaze processors implemented as partially reconfigurable tiles.

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2. TECHNIQUE AND RESULTS

The FPGA board features two Xilinx FPGAs. A Virtex-6 is the primary FPGA used for research designs. A Spartan-6 serves as a control and interface device between the Virtex-6 and the user. The board leverages the active partial reconfiguration, readback, and configuration scrubbing capabilities of the Virtex-6 through direct access to the device's configuration port. In a multicore system, active partial reconfiguration enables instantiation of computational resources, such as hardware accelerators, input/output interface cores, or microprocessors, on an as-needed basis at runtime without system interruption. A specific research problem of interest is the reduction of resource utilization by the interconnect among computational tiles in a multicore or multiprocessor FPGA system due to the complexity of the interconnect increasing with the number of cores A dedicated bus architecture is a fast, but inefficient implementation as each connection requires a unique set of wires. In an FPGA, this means that logic resources that could otherwise be used by logic cores are consumed by routing. This research seeks to leverage work done in network-on-chip (NoC) studies and apply it to dynamically allocated multicore FPGA computer architectures.

3. CONCLUSION

A custom FPGA-based research platform is presented. A research system implemented on this platform demonstrates the need for a NoC. The example system is a radiation tolerant reconfigurable computer designed and implemented on the research hardware. It features nine Microblaze processors implemented as partially reconfigurable tiles. Complexity in the inter-tile routing reduces the amount of logic resources available for computational use. A shared network layer is proposed as a way to alleviate the routing complexity and enhance the flexibility of the multi-tile system.