DesignConEast 2005

Design of a Low-Power Differential Repeater Using Low Voltage and Charge Recycling

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Abstract

Advances in System-on-Chip (SoC) design have emphasized the need for driving long on-chip differential traces. The delay of long traces has traditionally been handled by inserting repeaters at periodic intervals. The repeater method reduces the delay at the expense of increased power consumption. At the same time, power is a major design consideration in SoC design, motivating a driver methodology that has comparable delay to the repeater approach, with lower power consumption. This paper presents the design of a differential driver using low-voltage swing and charge recycling. The low-voltage design is shown to reduce the overall power by 37% and the Power-Delay-Product by 32% compared to traditional full-swing differential repeaters. By including charge recycling, the power can be reduced by 43%, which includes the power consumed by the associated control circuitry. This indicates that the charge recycling low voltage differential driver methodology is valuable when power is a major design concern.

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Brock J. LaMeres received his BSEE from Montana State University in 1998 and his MSEE from the University of Colorado in 2001. He is currently a Ph.D. candidate at the University of Colorado where his research focus is VLSI Circuit Design and High-Speed I/O for next generation IC's. For the past 7 years he has worked as a hardware design engineer for Agilent Technologies in Colorado Springs where he designs logic analyzer probes and acquisition boards. LaMeres has published over 30 technical articles in the area of signal integrity and holds a patent in the field of logic analyzer probing. LaMeres is a registered Professional Engineer in the State of Colorado.

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I. Introduction

The ever-decreasing feature size of VLSI circuits is allowing complex systems to be implemented on a single silicon substrate. As more system functionality is added to the silicon, the need to drive long interconnect traces is increased. This poses a problem for designers since the delays associated with long interconnect can severely limit system performance. Since both the resistance and capacitance of on-chip traces increase with length, the delay increases quadratically. To combat this, repeaters are inserted along the trace at periodic intervals. While this reduces the overall delay of the trace and allows the delay to scale linearly with trace length [1], it increases the system power. SoCs also have very tight power budgets since power is one of the major factors limiting Deep Sub-Micron (DSM) VLSI design. Long interconnects consume a large quantity of power, due to their large total capacitances. For example, it has been reported that the power consumption of the clock net for present-day designs is between 40-70% [2], [3]. Therefore, a repeater design technique which reduces power consumption is sought, even if such a technique has a minimal delay increase. By using a low-voltage output architecture, the power consumed by the repeaters can be reduced considerably.

Further, by implementing a charge recycling circuit, additional power savings can be achieved. In this paper, we describe our initial experimental results for such an on-chip, low voltage swing, differential repeater design which utilizes charge recycling technology. Charge recycling based drivers were recently described in [4] and [5]. However, the authors of these papers did not consider the use of low voltage swing charge recycling drivers. Also, only single drivers were considered. The contribution of this paper is to demonstrate the utility of charge recycling techniques in the repeater insertion context, where each charge recycling driver is a low voltage swing circuit. This circuit is for use on long traces that use differential signaling to overcome on-chip noise. We show that such charge recycling techniques can yield a repeater insertion solution with significantly reduced power consumption, with a small delay penalty.

The remainder of this paper is organized as follows. Section II describes the repeater design methodology commonly in use in contemporary designs. Section III describes the proposed repeater design methodology. Experimental results are reported in Section IV and conclusions are drawn in Section V.

II. Standard Repeater Design

When driving long interconnect traces on-chip, one way to reduce the delay is to insert repeaters along the trace. Figure 1 shows the standard repeater topology. By breaking the parasitic resistance and capacitance of the trace into smaller segments, the delay of the trace can be made to asymptotically approach zero as the number of segments increases. This is accompanied by an increase in the total repeater delay. Therefore the total delay has a minimum, which occurs for reasonable values of n, number of wire

segments. In previous work [6], an analytical expression was derived for the optimum value of n and the sizes of each of the repeaters.
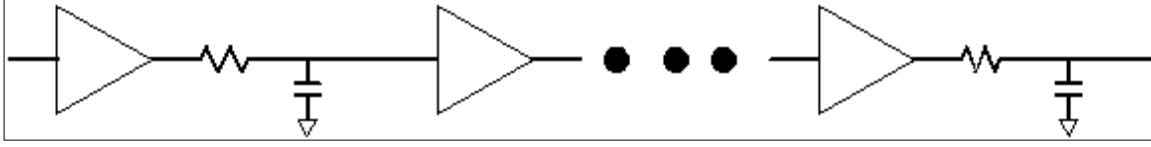

Figure 1. Standard Repeater Architecture

It can be shown that the optimal number of stages is found when the delay of the trace segment is equal to the delay of the repeater [1]. When implementing this technique, inverters are used as the repeaters. The optimal number of repeaters is rounded to the nearest even integer to preserve the logic function. When solving for the number of repeaters, the delay of the inverter is dependent on its channel width, power supply, and diffusion capacitance. Estimating the inverter delay using the integral-current method [7] and equating this to the trace segment delay can be written as:

$$\tau_{inv} = \tau_{RC_{trace}} \tag{1}$$

where,

$$\tau_{inv} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \cdot \left[\frac{2 \cdot V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4 \cdot (V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right] \tag{2}$$

$$\tau_{RC_{trace}} = (0.69) \cdot \left(\frac{R_{total}}{n}\right) \cdot \left(\frac{C_{total}}{n}\right) \tag{3}$$

When solving for the optimal number of repeater stages, C$_{load}$ in the inverter delay expression is the diffusion capacitance of the inverter output [1], [7].

$$C_{load} = C_{db,n} + C_{db,p} + C_{gd,n} + C_{gd,p} \tag{4}$$

Here the components of the load capacitance are respectively the diffusion capacitances of the NMOS and PMOS devices, and the gate capacitances of the NMOS and PMOS devices of the inverters.

Another existing approach utilizes boosters [8], [9] instead of repeaters. In this approach, the wire is not broken into segments (thus allowing for bidirectional transfers). Boosters have an early edge detection circuit, which augments the drive of a signal once a rising or falling edge is detected. Boosters improve the wire delay over repeaters, but the power requirements of boosters are higher than that of repeaters.

III.   Proposed Repeater Design

The drawback of a standard repeater method is that it consumes a significant amount of power in the inverter stages. One way to reduce the power and still reduce the delay of the trace is to implement a differential, low-voltage output stage with charge recycling.

A.   Differential Signaling

When driving long on-chip interconnect, differential signaling can be adopted as a way to reduce delay, improve noise immunity and enhance signal integrity [1], [8].   The differential driver architecture is implemented using complementary inverter stages [9]. The differential topology lends itself well to charge recycling that is discussed later. Figure 2 shows the topology of a differential buffer.
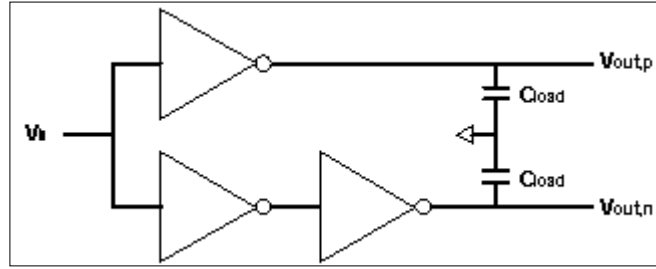

Figure 2. Differential Architecture

B.   Low-Voltage Output Swing

Charging and discharging long interconnect traces consumes a large amount of power in VLSI circuitry. The dynamic power associated with driving the output loads is expressed as:

$$P_{switching} = \alpha \cdot C_{load} \cdot V_{swing} \cdot V_{DD}^2 \cdot f \qquad (5)$$

where α is the switching activity. This expression illustrates that reducing the output voltage swing of the   driver (V_{swing}) results in a quadratic reduction in the power consumption of the circuit.

Figure 3 shows the proposed low-voltage inverter circuit. By inserting additional MOS transistors between V_{DD} and V_{SS}, the output swing is reduced. M1 and M2 perform the traditional CMOS inversion. M3 is an NMOS transistor whose gate is tied to V_{DD}. This has the effect of limiting the V_{OH} of the inverter to $V_{OH} = (V_{DD} - V_{T,n})$. M4 is a PMOS transistor whose gate is tied to V_{SS}. This limits V_{OL} of the inverter to $V_{OL} = (V_{SS} + V_{T,p})$.
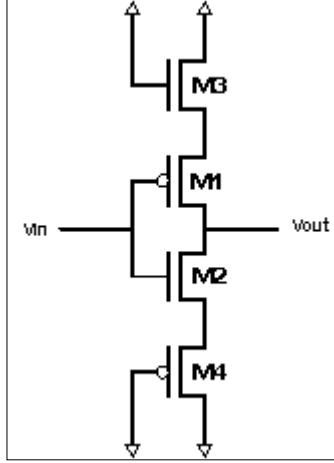
Figure 3. Low-Voltage Inverter

The new reduced output swing of the inverter is:

$$V_{LV_{swing}} = V_{DD} - V_{T,n} - |V_{T,p}| \tag{6}$$

This circuit is used for both the $V_{out,p}$ and $V_{out,n}$ signals of the differential driver described in the previous section.

C.   Charge Recycling

Additional power savings can be accomplished by implementing a charge recycling technique [4], [5], [9]. In charge recycling, the charge from one side of the differential pair can be used to charge the complement side when switching. This is accomplished by inserting an NMOS transistor between the output lines of the inverter. When the inverter switches, the output lines are momentarily shorted together using the NMOS transistor. The complementary lines exchange charge until they both reach an equal potential. At that point, the lines are isolated and the inverter completes the charging/discharging of the lines. This has the advantage that the inverter does not need to completely charge and discharge the lines to V_{OH} and V_{OL}. This reduces the power dissipated in the inverter circuit.

Without charge sharing, every transition requires the inverter to completely charge one side of the pair while the other is completely discharged. The energy dissipated within one complete cycle of a driver without charge sharing is given as:

$$E_{load} = C_{out,p} \cdot V_{swing}^2 + C_{out,n} \cdot V_{swing}^2 \tag{7}$$

Consider the situation when the signal $V_{out,p}$ is being charged, while $V_{out,n}$ is being discharged. With ideal charge recycling, the energy dissipation can be decreased to:

$$E'_{load} = V_{swing} \cdot \int_{V_{swing} \cdot \frac{C_{out,p}}{C_{out,p}+C_{out,n}}}^{V'_{OH}} C_{out,p} \cdot dv \qquad (8)$$

which can be rewritten as:

$$E'_{load} = C_{out,p} \cdot V^2_{swing} \cdot \frac{C_{out,p}}{C_{out,p} + C_{out,n}} \qquad (9)$$

In this expression, E' can represent either a full swing inverter using charge recycling or a low-voltage inverter as described in the previous section. In the case of a full swing inverter, $V_{swing}=V_{DD}$. In the case of a reduced swing inverter, $V_{swing} = V_{LV,swing}$, based on our design of the low voltage inverter circuit. A similar expression can be written for the case when signal $V_{out,p}$ is being discharged, while $V_{out,n}$ is being charged. The charge recycling topology is illustrated in figure 4.
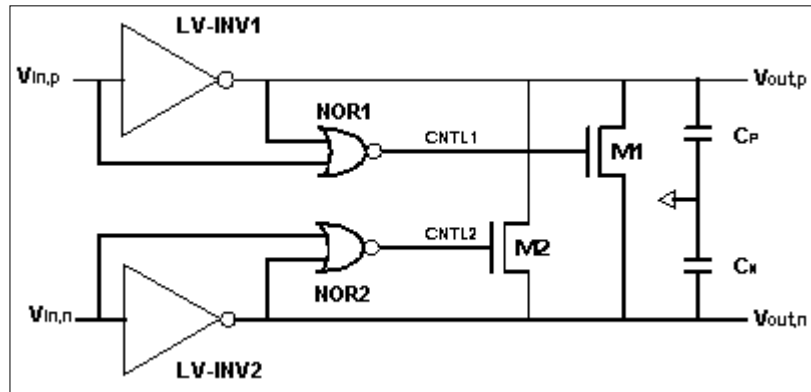

Figure 4. Differential Driver Using Charge Recycling.

This circuit implements a NOR-based charge sharing topology [9]. The NOR gates produce control signals to the charge sharing NMOS's (M1 and M2) that momentarily short the differential outputs together upon a transition. During the time that M1 or M2 is conducting, the charge from $C_{out,p}$ and $C_{out,n}$ is distributed equally between the two lines until the potential on each line is the same. At that point, the control signal is switched off and the CMOS inverter performs the remaining charging/discharging.

IV. Experimental Results

To evaluate the performance of the proposed method, simulations are performed using spice3f5 [10] with BSIM3 [11] model card support. A 0.1um CMOS process (obtained from the Berkeley Predictive Technology Model group [12]) was used for the simulations. The standard repeater technique is designed to drive a 1cm trace on metal 3 of this process using a nominal power supply of 3.3v. Three figures of merit - Power, Delay, and the Power-Delay-Product (PDP) - are recorded for this design. Then the proposed low-voltage and low-voltage with charge recycling topologies are used to drive the same 1cm line and their figures of merit are compared to the standard method.

For this comparison, the electrical values for the 1cm trace on metal 3 are found to be R=1333Ω and C=1.29pF [13]. By applying equations 1 through 3, the optimal number of repeaters for the standard topology was found to be 15. The optimal sizing for this topology was found to be (WP/WN)=(8um/2.5um). Using the same inverter sizing with the reduced voltage swing obtained from equation 6, the optimal number of low-voltage repeaters needed to drive this same 1cm trace is found to be 9. The number of low-voltage repeaters needed is less than the full-swing topology because the reduced output swing increases the inverter delay in spite of the reduced voltage swing (equation 2). We performed experimental sweeps of the number of segments, and verified that the theoretical numbers matched with the experimentally derived values.

Once the optimal number of low-voltage repeaters was found, the size of the low-voltage inverter transistors were swept to optimize for power and delay. Finally, the charge recycling circuitry was added to the low-voltage architecture to further reduce the power consumption. Figure 5 shows the total current that is drawn by the three repeater architectures. It should be noted that the low-voltage charge sharing current includes the NOR gate control circuitry. Clearly the two proposed designs consume much less power than the traditional full-swing repeater but suffer a small delay penalty.
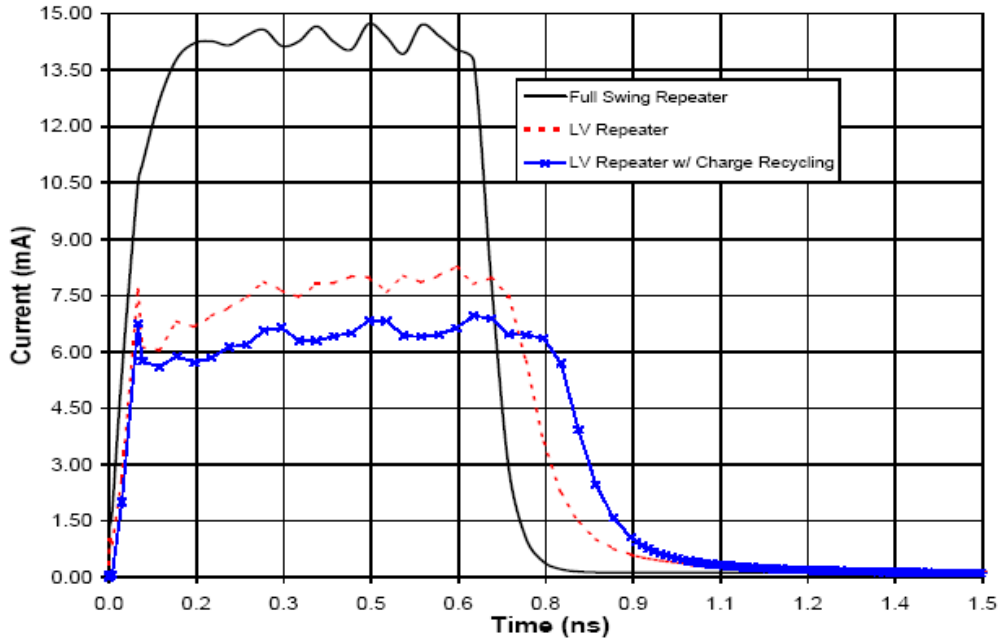
Figure 5. Repeater Current Profile Comparison

The efficiency of the low-voltage charge sharing circuit depends on the shape and timing of the control signals out of the NOR gates. If the control signals occur too soon relative to the driver transition, the charge sharing will turn off too early and limit the power savings. If the control signals occur too late, the output lines will still be shorted together when the inverter is trying to complete the charging/discharging. This causes the delay to increase. Figure 6 shows the control signals generated by the charge sharing circuitry.
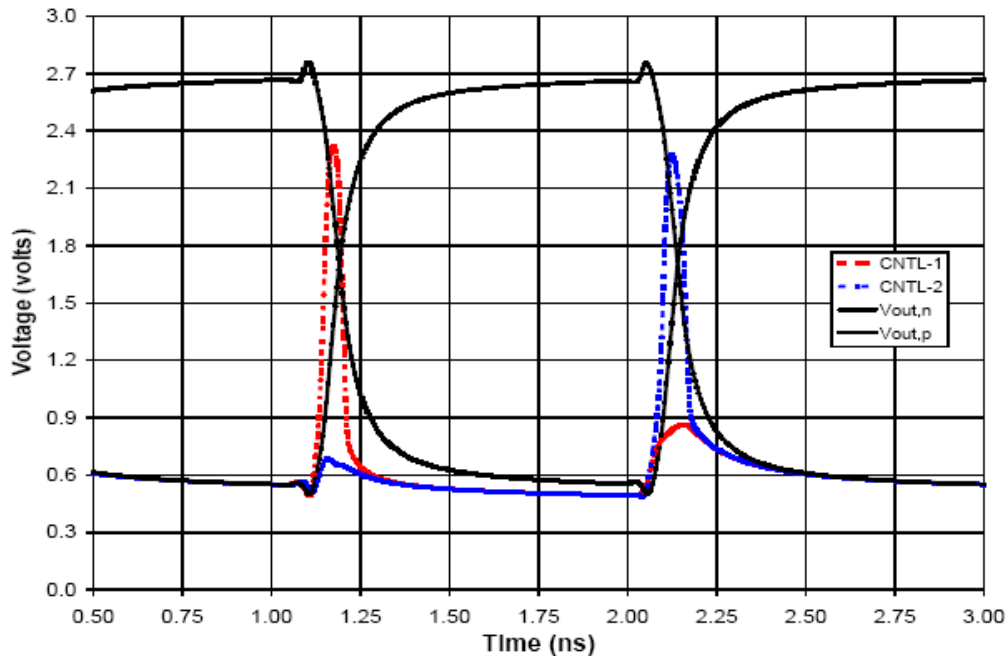

Figure 6. Charge Recycling Control Signals

Table I lists the results achieved between the three repeater architectures. The delay, power, and PDP are listed for each. In addition, the percentage improvement with respect to the full-swing repeater design are also provided. Note that the repeater with charge recycling has the lowest power consumption. Its delay is slightly increased over the low-swing repeater, with a very similar PDP compared to the low-swing repeater. Table II shows the sizing details for the three circuits.

Circuit	Figures of Merit			Improvement		
	Delay (ps)	Power (mV)	PDP (ps · mV)	Delay (%)	Power (%)	PDP (%)
Full-Swing Repeater	639	12.06	7.71	-	-	-
Low-Voltage Repeater	699	7.54	5.27	-9	37	32
Low-Voltage Charge Recycling Repeater	774	6.92	5.36	-21	43	31

Table I. Experimental Results for the Three Repeater Architectures Studied

Circuit	Section	Transistor	Size
Full-Swing Repeater	INV	NMOS	2.5/0.1
		PMOS	8.0/0.1
Low-Voltage Repeater	INV	NMOS	5.0/0.1
		PMOS	16.0/0.1
	V_t Drop	NMOS	25/0.1
		PMOS	80/0.1
Low-Voltage Charge Recycling Repeater	INV	NMOS	5.0/0.1
		PMOS	16.0/0.1
	V_t Drop	NMOS	25/0.1
		PMOS	80/0.1
	NOR	NMOS	0.2/0.1
		PMOS	0.8/0.1
	CS	NMOS	0.2/0.1

Table II. Transistor Sizes (Width/Length in *um*)

V.   Conclusion

In this paper, we have presented a low-voltage repeater with charge recycling that yields a significant improvement in power consumption with a small delay penalty. It was shown through simulations that by using a low-voltage output repeater design, the power consumed when driving a 1 cm, metal-3 trace could be reduced by 37% compared to a traditional full-swing repeater system. This power savings comes with only a 9% increase in delay yielding an overall PDP improvement of 32%. With the addition of a charge recycling stage on the low-voltage output, the power savings can reach 43% over the traditional approach. The low-voltage charge recycling circuit increased the delay by 21% but the net PDP was still improved by 31%.

We propose that this architecture be used as an alternative to full-swing repeater insertion when the design is more sensitive to power and can withstand a minimal increase in delay. In addition, this architecture is well suited for long traces that are using differential signaling to overcome on-chip noise.

References

[1]   W. Dally and J. Poulton, *Digital Systems Engineering*, Cambridge University Press, Cambridge, U.K., 1998.

[2]   H. Kawaguchi and T. Sakurai, "A Reduced clock swing flip-flop (RCFF) for 63% power reduction",   IEEE Journal of Solid-State Circuits, vol. 33, pg. 807-811, 1998.

[3]   T. Sakurai, "Design challenges for 0.1um and beyond", Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC), pg. 553-558, 2000.

[4]   E.D. Kyriakis-Bitzaros and S.S. Nikolaidis, "Design of Low Power CMOS Drivers Based on Charge Recycling", Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS), pp. 1924-1927, 1997.

[5]   X. Wang and W. Porod,   "A Low Power Charge-Recycling {CMOS} Clock Driver", Proceedings of the Ninth Great Lakes Symposium on VLSI, pp. 238-239, 1998.

[6]   V. Adler and E. Friedman, "Repeater design to reduce delay and power in resistive interconnect", IEEE Transactions Circuits Systems II, pp. June, vol. 45, pp. 607-616, 1997.

[7]   S. Kang and Y Lebledici, *CMOS Digital Integrated Circuits*, 2nd edition, McGraw-Hill Companies, 1999.

[8]   M. Purandare and A. Sung and S. Khatri, "A Differential Amplifier Based Technique to Reduce Delay in Long Interconnect", International Conference on VLSI Design, Mumbai, India, 2004.

[9]   I. Bouras and Y. Liaperdos and A. Arapoyanni, "A High Speed Low Power CMOS Clock Driver using Charge Recycling Technique", Proceedings of the IEEE Int. Symposium on Circuits and Systems (ISCAS), pp. 657-660, 2000.

[10]   L. Nagel, "SPICE: A Computer Program to Simulate Computer Circuits", University of California, Berkeley UCB/ERL Memo M520, May, 1995.

[11]   "BSIM3 Homepage", www-device.eecs.berkeley.edu/~bsim3/.

[12]   "BPTM Homepage", www-device.eecs.berkeley.edu/~ptm/.

[13]   A Nalamalpu and W Burleson, "Repeater insertion in deep sub-micron CMOS: Ramp based analytical model and placement sensitivity analysis", Proc. IEEE Symp. Circuits and Systems, 766-769, May, 2000.