RadSat - Radiation Tolerant SmallSat Computer System

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ABSTRACT

This paper describes the development of a SmallSat computer system that provides increased tolerance to radiation induced faults through a novel architecture implemented on commercial-off-the-shelf (COTS) Field Programmable Gate Arrays (FPGA). The computer system provides increased reliability, computational performance, and power efficiency at a fraction of the cost of existing radiation-hardened computer systems. This computer technology has had its technical readiness level steadily increased over the past 8 years through a variety of tests and flight demonstrations. These include high energy particle bombardment at the Texas A&M Radiation Effects Facility, 8 high altitude balloon flights to 30km, and a 2014 sounding rocket flight to 120km. The technology was selected by the NASA SmallSat Technology Partnership program in 2013 as one of the cross-cutting technologies that will enable advanced computing in small satellites and is being matured for even more rigorous flight demonstrations. These include a second sounding rocket flight to an altitude of 300km followed by a 6 month low earth orbit demonstration on the International Space Station, both in 2016. This computer technology was selected by the 2015 NASA CubeSat Launch Initiative for a long term stand-alone mission in Low Earth Orbit (LEO) in 2017.

INTRODUCTION

RadSat is the name of a satellite mission to demonstrate a novel computer architecture designed to mitigate radiation induced faults using COTS FPGAs. The computer technology is implemented as an experiment within RadSat to demonstrate it in an operational space environment. The fault mitigation approach in this computer involves breaking a commercial FPGA fabric into redundant tiles, each with the characteristics that they can fully contain the circuit of interest and also be individually reprogrammed using partial reconfiguration. Currently, each tile contains a full computer system based on a Xilinx MicroBlaze soft processor. At any given time, three of the tiles run in triple modular redundancy (TMR) with the rest of the tiles reserved as spares. The TMR voter is able to detect faults in the active triad by voting on the tile outputs. A configuration memory scrubber continually runs in the background and is able to detect faults in the configuration memory of both the active and inactive tiles. In the event of a fault in the active triad, (either detected by the TMR voter or scrubber), the damaged tile is replaced with a known good spare and foreground TMR operation continues. The damaged tile is repaired in the background by reinitializing its configuration memory through partial reconfiguration. Faults detected in inactive tiles by the scrubber are also repaired in the background and reintroduced as spares. This approach mitigates single event effects (SEEs) in the FPGA circuit fabric in addition to SEE's in the configuration memory. The advantage of this approach is that foreground operation can continue while faulted tiles are repaired and reintroduced into the system in the background. Since bringing on a spare tile takes significantly less time than performing background repair via partial reconfiguration of the damaged tile, the system availability is increased. This approach has been shown to improve the mean-time-before-failure compared to TMR+scrubbing alone. This computer architecture has been demonstrated on a Xilinx Virtex-6 FPGA with 9-tiles. For the final RadSat mission, the architecture will be implemented on a Xilinx Artix-7 FPGA with 4-tiles. More details on this technology can be found in [1-7].

MOTIVATION

Technology Relevance to NASA

The NASA Earth Science Decadal Survey states the need for on-board processing and power efficiency that far exceeds existing computer systems in order to meet NASA's future science goals [8]. Additionally, the problem statement for the flight computing needs within the NASA TA11: Technology & Processing Roadmap is "ultra-reliable, radiation hardened platforms which, until recently, have been costly and limited in performance" [9]. The TA11 roadmap also calls for innovative computing architectures to meet the needs of both science and engineering and emphasizes the need for scalable processing platforms that include intelligent fault-tolerant technologies to increase the robustness of computing platforms for long-duration missions. Simultaneously, the 2014 NASA Strategic Plan calls for "transforming NASA's missions and the Nation's capabilities by maturing crosscutting and innovative space technologies" (Objective 1.7), particularly those that decrease cost and thus expand opportunities for future space activities [10].

The NASA Strategic Plan also highlights one of its main activities to achieve its goals is "moving forward with critical research and technology demonstrations on the ISS" [10]. With the prevalence of computer systems in all future NASA missions, improving the capability of space computers has significant relevance and broad-scale impact across all NASA programs. Using commercial off-the-shelf (COTS) field programmable gate arrays (FPGAs) to implement space computer systems has the greatest potential to increase on-board processing and power efficiency while at the same time providing platform scalability and reduced cost. Using COTS FPGAs allows increased computation and power efficiency by taking advantage of advances in commercial fabrication processes. Implementing a radiation fault mitigation strategy on FPGAs provides reliability while at the same time drastically reduces the cost of space computing through the use of COTS parts.

Radiation Effects on Space Computers

Space computers must operate in a harsh radiation environment that leads to multiple types of failures. Radiation effects are separated into two broad categories: Total Ionizing Dose (TID) and Single Event Effects (SEE) [11-12]. Each of these failure mechanisms are caused by ionizing radiation striking the integrated circuit substrate and depositing unwanted energy. TID failure is caused by lower energy protons and electrons ($\leq$30MeV/amu) striking the substrate and creating electron/hole pairs that are trapped in the insulating materials of the electronic devices. When this trapped charge occurs in the gate oxide of a transistor it causes the threshold voltage to be altered, which leads to input leakage current and eventually puts the device into a state where it is either always on or always off. When this trapped charge occurs in the isolation regions between devices, it can cause leakage current that consumes excessive power and can ultimately destroy the device. TID exposure causes a gradual degradation of the part as opposed to instantaneous failure. The following figure shows the cross-section of typical MOSFET device and how various radiation strikes cause different types of failures.
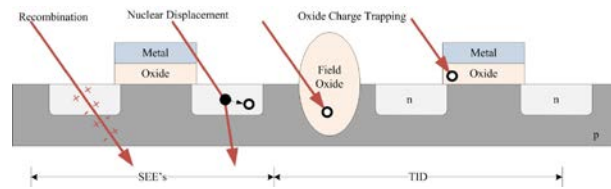

Figure 1: Cross-Section of a MOSFET Device Showing Radiation Fault Mechanisms.

SEE faults refer to electron/hole pairs caused by high energy particles and heavy ions striking the diffusion regions of a device. SEEs do not cause permanent damage to the device like TID does, but they do cause unwanted logic level transitions. These unwanted transitions lead to logic system failures such as erratic computer behavior or full system crashes. When a high-energy particle passes through an integrated circuit and generates enough free charge carriers to change the state of a digital logic line, it is called a single event transient (SET). If this voltage transient is captured and stored by a flip-flop or other memory device, the event is referred to as a single event upset (SEU). It is generally possible to recover from an SEU by simply resetting the affected circuit. However, if the SEU somehow produces such an alteration that a reset alone is not sufficient to restore the device to a healthy state, it is called a single event functional interrupt (SEFI). SEFI's typically require more drastic recovery measures such as power cycling or full system re-initialization.

Historically, the feature sizes of integrated circuits used to implement space computers were such that TID was the primary concern with respect to radiation. Larger devices had thick oxide insulators that were highly susceptible to charge trapping because of their relatively large volumes within the device. Simultaneously, the diffusion regions of the older devices where large enough that a high energy particle strike did not cause sufficient energy in order to change the state of a logic gate. This was because the radiation

particles sizes were relatively small compared to the diffusion region volume and a strike could not create a sufficient amount of charge to switch the device. In modern integrated circuits (e.g., below the 65um process node), the feature sizes have been reduced to the point where TID is no longer the dominating failure mechanism. This is because the oxide thicknesses of the devices are so thin that the statistical probability of charge getting trapped is minimal. Thus, modern ICs are becoming inherently tolerant to TID. For example, modern FPGAs are achieving TID tolerance levels >300krad when implemented in the 65nm process node and as much as 600krad when implemented in a 22nm node [13]. As TID immunity is increased with each subsequent process node, so is the susceptibility to SEEs. In modern devices, faults caused by SEEs are now the greatest concern [14]. This is because the diffusion regions of modern devices have been reduced in size to the point where the charge caused by a radiation strike is sufficient to cause a state change. What makes SEEs even more concerning is that the energy levels are significantly high that shielding is not practical. To stop all high energy particles capable of causing SEEs in modern devices it would require an aluminum shield a meter thick. Furthermore, the energy levels of these particles are so high that they cannot be reproduced on Earth. This means that solutions to mitigate faults caused by SEEs can only truly be evaluated in a space environment.

While modern FPGAs are a highly attractive platform for space computing due to their low cost, performance, flexibility, and increased TID immunity, they are uniquely susceptible to SEEs [15]. An FPGA stores the data that represents its current hardware configuration in banks of SRAM inside the device. SEUs that occur within this SRAM alter the circuit configuration of the FPGA. Such faults cannot be corrected by a simple reset since the circuit itself is changed by the SEU. Therefore, SEFIs are far more common in SRAM-based FPGAs than in traditional integrated circuits. SEFI's require the configuration SRAM to be reinitialized before the circuitry can then be reset and continue operation. Additionally, FPGAs are susceptible to SETs and SEUs in their circuit fabrics just as any other digital device. This means that any FPGA used to implement a space computer must have a strategy for mitigating all SEEs including SETs, SEUs, and SEFIs.

Existing Approaches to Radiation Hardened/Tolerant Space Computing

There are three common techniques that have historically been used to mitigate TID in space computers. The first is to use non-standard layout techniques in order to minimize the probability of charge getting trapped in the insulating materials of the

devices. This technique, known as radiation-hardened-by-design (RHBD), uses approaches such as enclosed-layout-transistors and guard rings in order to minimize the area of susceptible insulating regions and provide safe conduction paths for radiation induced charge carriers to flow instead of being trapped in the insulating materials [16]. The second historical technique to mitigate TID is to use non-standard materials in the fabrication process. This technique, known as radiation-hardened-by-process (RHBP), fabricates the devices with materials that are less susceptible to charge trapping and produce fewer electron/hole pairs during a radiation strike. These techniques have achieved TID tolerance in the range of 300krad-1Mrad [17].

There are a variety of drawbacks of using RHBD and RHBP TID mitigation techniques [18]. First, the techniques require additional circuit area, thus the performance and power efficiency is less than devices fabricated in the same node using standard design approaches. Second, since the fabrication procedures are custom and the part volumes are low, it leads to extremely expensive computer systems. For example, radiation hardened processors such as HyperX, Maestro, and the RAD6000 can cost as much as 40x greater than commercial equivalents and only achieve computation rates up to 35 MIPs [9]. The BAE RAD750 radiation-hardened processor has achieved performance rates up to 200 MIPs but also has a similar cost and consumes up to 20W for the full computer system [19]. Radiation hardened processors typically lag behind commercial equivalents by approximately 10 years in performance (see figure 2) [20]. This performance gap in addition to the high cost of custom, radiation hardened processors has created a new demand for space computers that use novel approaches to radiation tolerance.
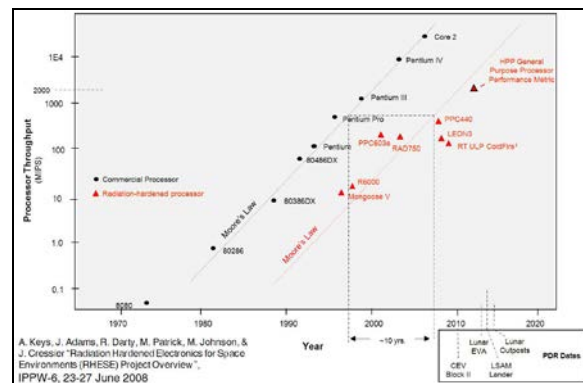

Figure 2: Performance Comparison between Radiation-Hardened and COTS Processors [20].

The third historical technique to mitigate TID is to use shielding. There are also a variety of drawbacks of using shielding to mitigate TID including increased mass and the inability of shielding to stop higher energy radiation. The following figure shows the dose rate that will make it to a circuit substrate for varying thicknesses of aluminum shielding [21]. The plot shows the results for the typical TID causing radiation experienced in LEO. This plot illustrates that there is a diminishing return in the amount of protection that is provided by shielding for thicknesses above ~0.15". The total dose reaching the circuit, comprised mainly of protons (~30MeV/amu) is not significantly reduced even when the shielding thickness is doubled. Shielding inefficiency becomes even more pronounced for higher energy radiation (100MeV-1GMeV). Since adding mass to a space mission is extremely expensive, the use of excessive shielding is an unattractive technique and new measures to radiation tolerance are needed.
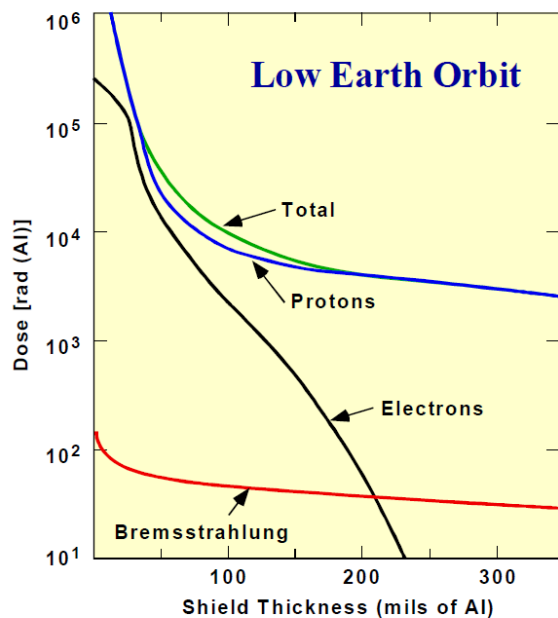

Figure 3: Effective Dose Rate vs. Aluminum Shielding Thickness in LEO [21].

Existing SEE mitigation strategies fall broadly into two categories: (1) redundancy and (2) memory *scrubbing* [22]. The most commonly adopted form of redundancy is triple modulo redundancy (TMR) [23]. TMR involves triplication of the computing hardware and adding a voting circuit to compare the outputs of the three hardware modules. In the event of an SEE fault in one of the circuits, two of the circuits are still operating properly. The voter will produce the final system output based on the majority of the three circuits (e.g.,

the two properly operating circuits), thus creating a final output that was not affected by the SEE. In the event of an SEU, a recovery procedure is typically needed after the final result is produced in order to put the faulted circuit back into an operational state. If the fault was created by a SEFI, an even more sophisticated recovery procedure is needed. The following figure shows the typical TMR topology.
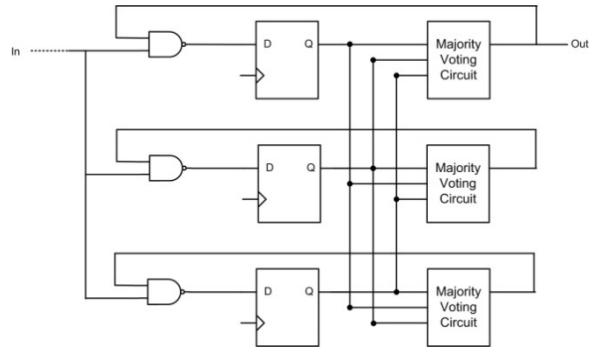

Figure 4: Triple Modulo Redundancy

Memory scrubbing is the process of continually checking the contents of memory for failures by either comparing it to a known good copy (for the cases of configuration or program memory) or comparing it to redundant memory components (for the case of variable memory) [24]. When scrubbing configuration or program memory, the system requires a radiation-safe, non-volatile memory device for storing the golden copy that is often implemented using either PROMs or EEPROMs that are more SEE immune but un-writable during normal operation. For space computers implemented on FPGAs, scrubbing of the configuration memory must be done continually in order to detect and recover from SEFIs.

While TMR and scrubbing are widely accepted SEE mitigation techniques, they have multiple drawbacks that should be addressed for increased reliability. First, TMR protects against instantaneous errors, but its reliability decreases as the length of the mission grows and the probability of faults in multiple modules increases due to the additional circuit area of the triplication; in fact, TMR becomes less reliable than simplex systems after a certain mission time has been exceeded [23]. Scrubbing, on the other hand, prevents errors from accumulating, but cannot always correct recent errors fast enough to prevent bad outputs. The latency between the occurrence of a fault in configuration memory and detection by the scrubber can be significant due to the sequential manner that the scrubber traverses the configuration memory [24].

OUR CONTRIBUTION TO SPACE COMPUTING

Montana State University (MSU) has been researching an architecture that improves the state-of-the-art in space computing by deploying a novel SEE fault mitigation architecture on modern COTS FPGAs. Using a COTS FPGA fabricated in a process node of 45nm yields an acceptable level of TID immunity inherently through minimal feature sizes (~400krad). The use of a modern COTS FPGA also provides a significant increase in computational performance and power efficiency compared to custom, radiation hardened processors that use RHBD or RHBP techniques. The use of a COTS FPGA produces a tremendous reduction in cost by avoiding using low-volume, custom, radiation-hardened parts. MSU's novel SEE mitigation architecture (details below) improves reliability beyond TMR+Scrubbing in order to deliver a platform that addresses all of NASA's priorities for next generation space computers.

MSU's SEE fault mitigation approach extends TMR+Scrubbing by including spare circuitry to enhance the operation of TMR and a spatially aware approach to improve traditional scrubbing. MSU's approach to providing reliability involves breaking a commercial FPGA fabric into redundant tiles, each with the characteristics that they can fully contain the circuit of interest and also be individually reprogrammed using partial reconfiguration. For purposes of demonstration, each tile contains a Xilinx MicroBlaze soft processor (32-bit RISC architecture provided by Xilinx). At any given time, three of the tiles run in TMR with the rest of the tiles reserved as spares. The TMR voter is able to detect faults in the active triad by voting on the tile outputs. A configuration memory scrubber continually runs in the background and is able to detect faults in the configuration memory of both the active and inactive tiles. In the event of a fault in the active triad, (either detected by the TMR voter or scrubber), the damaged tile is replaced with a known good spare and foreground TMR operation continues. The damaged tile is repaired in the background by reinitializing its configuration memory through partial reconfiguration. This approach mitigates SEUs in the FPGA circuit fabric in addition to SEFIs in the configuration memory. The advantage of this approach is that foreground operation can continue while the faulted tile is repaired and reintroduced into the system in the background. Since bringing on a spare tile takes significantly less time than performing background repair via partial reconfiguration of the damaged tile, the system availability is increased. This approach has been implemented on a Virtex-6 LX75-1 FPGA with 9 MicroBlaze soft processors. The following figure shows a prototype Virtex-6 FPGA board that has been developed at MSU and the FPGA floor plan of the 9-tile MicroBlaze system. Each square within the floor plan represents a tile that contains a full 32-bit MicroBlaze soft processor and can be partially reconfigured.
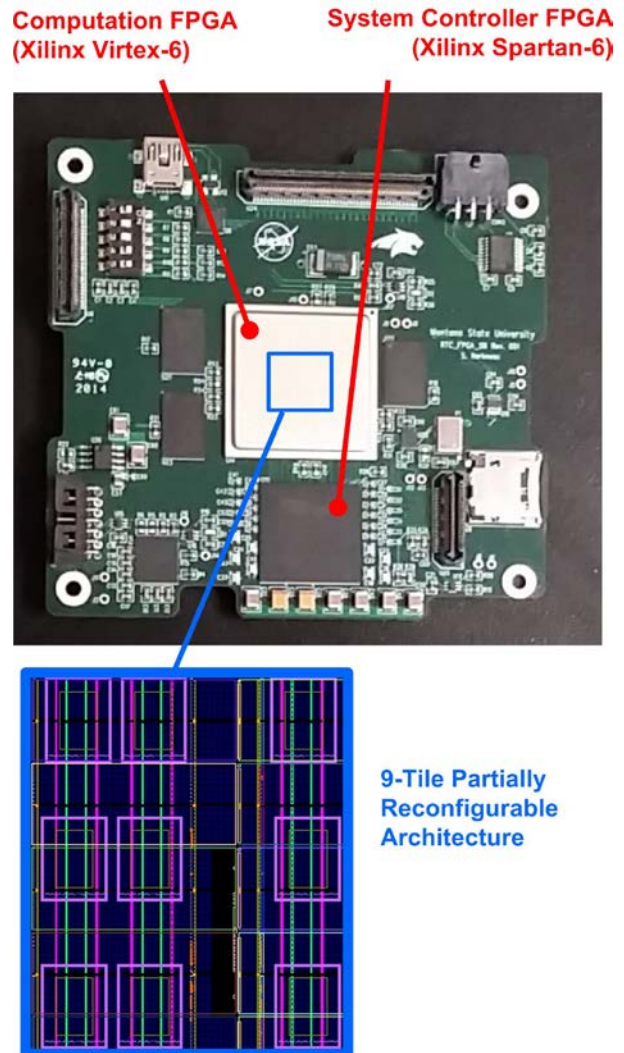

Figure 5: FPGA Board and Fabric Layout of Partially Reconfigurable Architecture.

In order to theoretically analyze the reliability of the SEE mitigation strategy, a Markov model was used. A Markov model describes a system as a directed graph, in which each node is a state and each edge represents a transition between states. The states traverse between "Good" and "Failed" based on incoming faults and fault recovery. For systems with the ability to recover from a fault (e.g., TMR, Scrubbing, Spares), there are one or more intermediate states in the graph that allow the system to continue operation in the presence of a fault. The timing of the transitions through the graph are dictated by the fault rate (e.g., incoming radiation) and the repair rate (e.g., scrubbing and/or circuit

replacement). The following figures show the Markov chains for three FPGA-based computer systems. The first chain represents a single MicroBlaze processor implemented on a Virtex-6 FPGA with no fault mitigation strategy. This is the "Non-Redundant" system and will fail when a radiation induced fault occurs in a sensitive region. The second Markov chain is the typical fault mitigation approach used on FPGA-based MicroBlaze space computers (e.g., TMR+Scrubbing). This system can tolerate a single fault in its triad and will recover as long as the error is corrected by the scrubber before another fault occurs in one of the other active circuits. The last Markov chain improves upon TMR+Scrubbing by including 6 spare circuits (e.g., the MSU approach). The spare circuits allow the system to withstand more radiation faults before failing by reducing recovery time. This system also has the ability to partially reconfigure damaged tiles in the background and reintroduce them into the system as spares. This is the "TMR+Scrubbing+Spares" system.
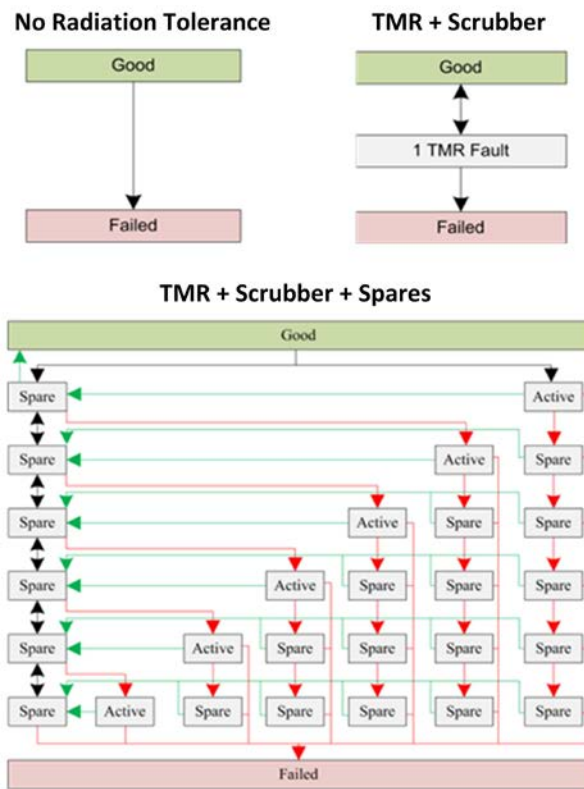

Figure 6: Markov Chains used to Compare SEE Mitigation Approaches.

The rate to replace a damaged tile with a spare was determined empirically on the Virtex-6 at 1ms. The rate to repair a damaged tile via scrubbing was determined empirically on the Virtex-6 at 100ms. The following figure shows the availability of each system

as a function of the incoming fault rate. The availability is the percentage of the time that the foreground operation is doing computation, as opposed to waiting for or performing repair. This plot illustrates how a TMR+Scrubbing+Spare system delivers significantly more computation architecturally compared to the other systems.
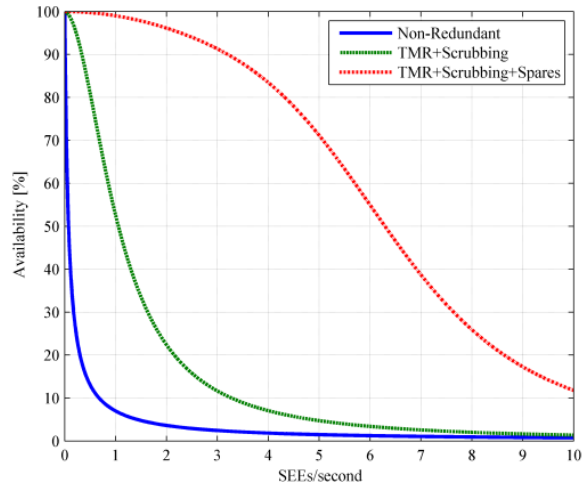

Figure 7: Availability of Different FPGA Fault Mitigation Approaches.

In order to determine the system's reliability in a representative environment, fault rates for the Markov model were extracted from the CREME96 tool for a LOE orbit [25]. The space weather environment was set for the worst week, solar flare conditions. CREME96 considers both the radiation strike rate but also the linear energy transfer of the device when predicting SEEs. The resource utilization is then factored to find the design specific SEE rate [26]. As expected, the highest fault rate was experienced in the South Atlantic Anomaly (SAA) at 1.1 SEEs/second. This corresponded to related data in [27] and [28]. In [27], a Virtex-4 FPGA-based computer developed by the Goddard Space Flight Center (GSFC) and deployed on MISSE-7 experienced 0.1 SEEs/day averaged across the entire ISS orbit under normal weather conditions. The following figure shows the probability of a failure based on the hours of operation in the worst case ISS environment (e.g., the SAA). From this plot, the Mean-Time-Before-Failure (MTBF) can be extracted, which is defined as the point at which the probability of failure is 50%. This figure shows that the TMR+Scrubbing+Spares approach achieves a significantly longer MTBF compared to the traditional TMR+Scrubbing approach (5.4 hours vs. 3.6 minutes). This analysis verifies that the proposed system dramatically increases the reliability over existing fault mitigation strategies by a factor of 90x. In the event of

a more severe radiation environment (e.g., peak 5 minutes of a solar storm) that has a fault rate with the potential to overrun the MSU system and causes a system failure, a 2-minute watch dog timer is included that will trigger a full FPGA reconfiguration.
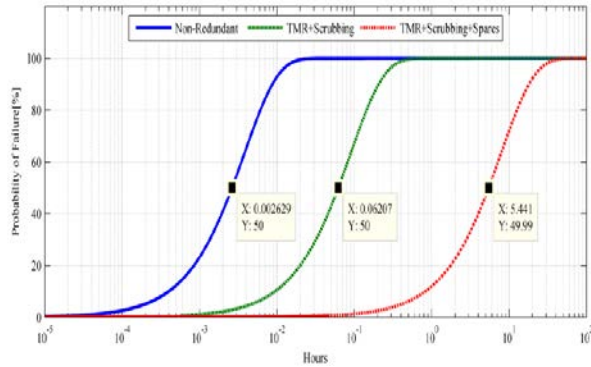

Figure 8: Failure Probability of Different FPGA Fault Mitigation Approaches.

Another novel contribution of the MSU system is the use of a spatial radiation sensor that is coupled with the FPGA to reduce the latency between a fault occurrence and repair by the scrubber. MSU has developed a sensor that detects the spatial location of ionizing radiation with energy levels capable of causing single event faults in modern FPGAs [29]. This technology uses a wide area, vertical p-i-n junction as the sensing element. The top and bottom sides of the silicon die contain strips of electrodes that are orthogonal to each other. As radiation passes through the sensor, it creates electron-hole pairs in the depletion region of the p-i-n junction. Due to the built-in electric field of the junction, electrons are swept to the top side and holes are swept to the bottom side. The electrodes collect the excess charge and allow the XY location of the strike to be detected by observing the intersection of the current pulses. A p-i-n structure is used so that it takes less voltage to fully deplete the sensing element (+14v) compared to typical p-n detectors that takes as much as +50v to fully deplete [29]. The current pulses from the electrodes are amplified, digitized and sampled. This information is used by the control system for the FPGA to provide yet another layer of fault mitigation. Strikes in active tiles will cause a spare processor to be brought online. Strikes in inactive spares will cause the scrubber to repair the tile before it is brought online, which keeps more good spares available to the system. The size of the MSU sensor is 20mm x 20mm, which is large enough to cover any commercial FPGA die. The sensor has 256 discrete detection pixels, which gives numerous pixels within each tile. The following figure shows a montage of information about the radiation sensor that has been developed at MSU.
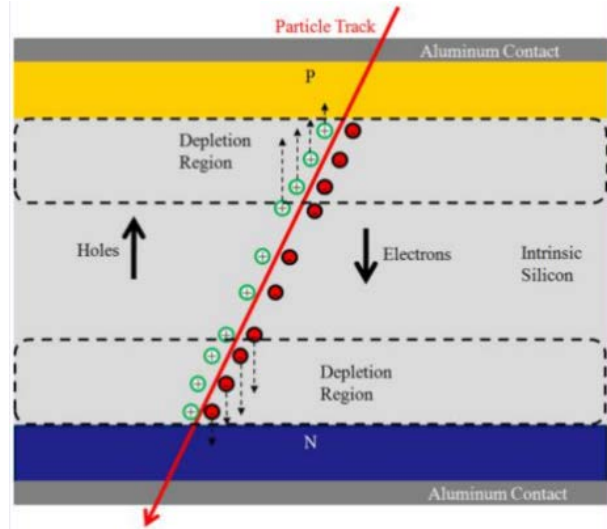

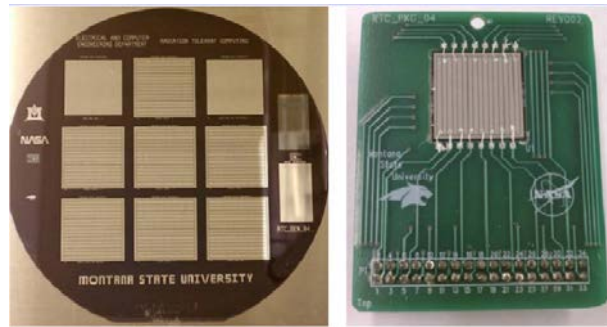**Figure 9: Cross-Section of Radiation Sensor.**

Figure 10: Sensor Implementation.

This computer implementation using a Xilinx Virtex-6 LX115-1 FPGA has achieved performance of 234 MIPs at 2W of full system power consumption. This represents a 2x improvement in power efficiency compared to the RAD750 and a 7x increase in performance compared to the more widely adopted radiation hardened processors (e.g., HyperX, Maestro, RAD6000). The Virtex-6 uses a 45nm process node that has been shown to provide up to 380krad (1 Mrad with reduced timing) [14] of TID immunity, which meets the TID requirements for the majority of space missions [30]. The novel SEE mitigation strategy of our computer extends the SEE immunity of a COTS Virtex-6 FPGA beyond existing mitigation strategies by a factor of 90x. The Mean-Time-Before-Failure due to SEE's on the Virtex-6 of the proposed system in the worst case ISS orbit (e.g., the SAA) under worst week conditions is 5.4 hours compared to only 3.6 minutes using existing mitigation strategies (e.g., TMR+Scrubbing). This computer system promises to meet the performance, power efficiency, and reliability requirements of future science missions at a cost that is 100x lower than existing radiation hardened computers.

COMPUTER TECHNOLOGY MATURATION

This section gives a brief history of the maturation of this computer technology. The computer experiment within RadSat has been matured from TRL-1 in 2007 to its current level of TRL-6 through a variety of demonstrations. With each demonstration, the computer system has been implemented in different form factors and different levels of complexity. Between 2008 and 2010, a prototype of this computer system was implemented using commercial FPGA evaluation boards. These boards, in conjunction with prototype boards, allowed the concept to be matured to TRL-2 and TRL-3 through numerous demonstrations to engineers from the Marshall Space Flight Center. Engineers from MSFC traveled to MSU four times during this period to evaluate the technology. MSU faculty and students also traveled to MSGC three times to demonstrate the computer system. The following figure shows the computer technology proof of concept prototype that was used to demonstrate TRL-3.

Figure 11: Prototype Hardware used to Demonstrate TRL-3.

In 2010, the computer technology was implemented in a 4"x4"x4" cube form factor to facilitate testing under radiation bombardment in a cyclotron. Between 2010 and 2011 the computer system was tested twice at the Texas A&M Radiation Effects Facility while being bombarded with the ion Kr at 25 MeV/AMU. The computer system demonstrated an integration of technology components and validation in a laboratory environment to achieve TRL-4. The following figure shows the computer system in its TRL-4 form factor and the test apparatus used to place the computer system in the beam of the cyclotron.
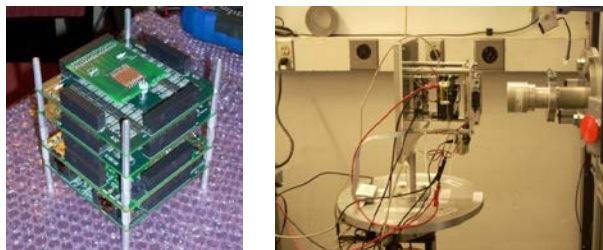

Figure 12: Prototype Hardware used for Cyclotron Testing and Demonstration of TRL-4.

After the cyclotron demonstrations, the computer technology was implemented in a form factor that supported high altitude balloon flight testing. A stand-alone power supply was designed and integrated with the computer system in addition to a data logging system. Between 2011 and 2013, the computer technology was flown on eight high altitude balloon missions. Six of the balloon flights were conducted by the Montana Space Grant Consortium's BOREALUS program to altitudes of 90,000 feet in southwest Montana. Two of the balloon flights were conducted by NASA's Columbia Scientific Balloon Facility to altitudes of 120,000 feet over New Mexico and Arizona. This validated the technology in a relevant environment and demonstrated TRL-5. The following figure shows a montage of images associated with the TRL-5 balloon flight demonstrations.
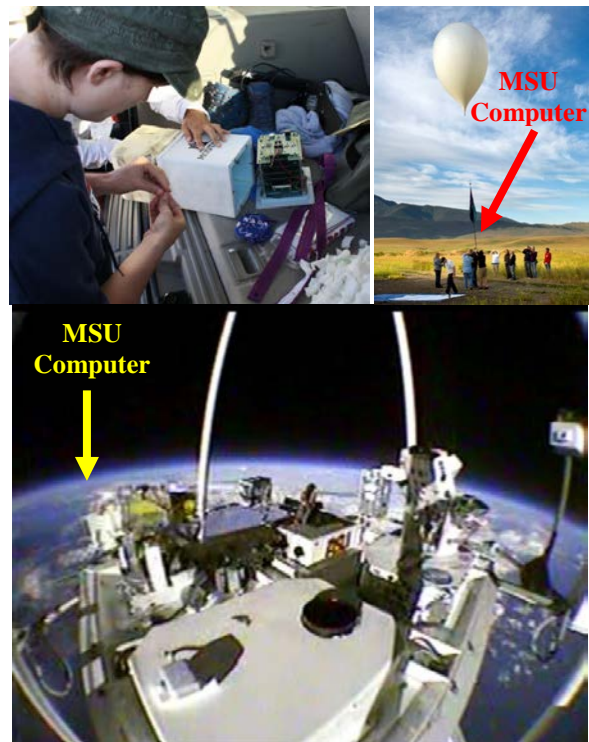

Figure 13: Computer Hardware and Flight Configuration used to Demonstrate TRL-5.

After the balloon tests, the computer system was implemented in a form factor that supported more rigorous flight testing. Between 2013 and 2014 the computer was redesigned in a standard 1U CubeSat format ($100cm^3$) and coupled with more advanced stand-alone power system. In 2014 the computer technology was flown on the SL-9 suborbital vehicle from UP Aerospace LLC to an altitude of 408,000 feet.

This flight validated the operation of prototype subsystems in a relevant end-to-end environment to demonstrate TRL-6. This rocket flight could have demonstrated TRL-7, but some hardware failures within the computer prevented a demonstration of the full system. The computer is scheduled to be flown again on the sounding rocket in 2015. The following figures show a montage of images associated with the TRL-6 demonstration.
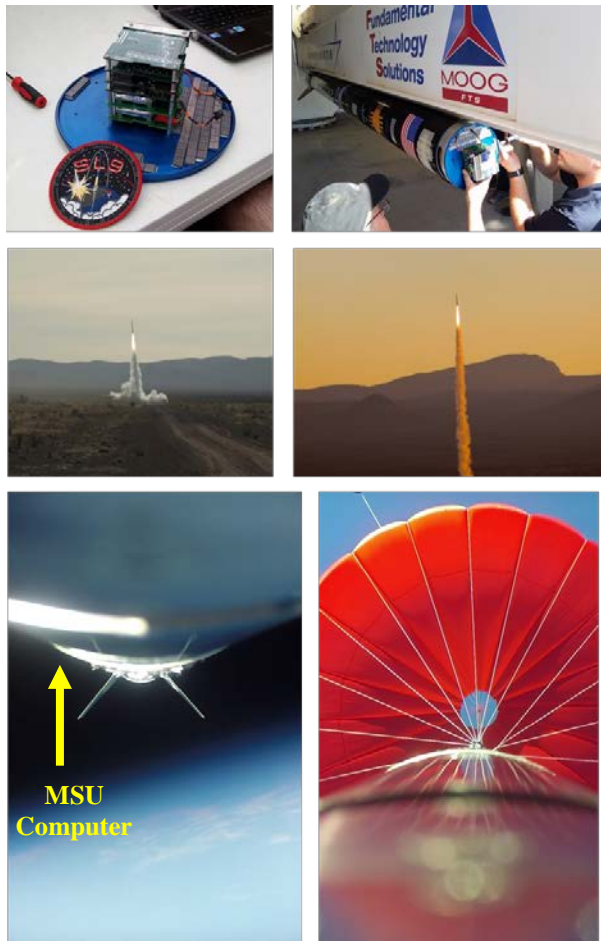

Figure 14: Computer Hardware and Flight Configuration used to Demonstrate TRL-6.

RADSAT MISSION CONCEPT

Satellite Architecture

The purpose of the RadSat mission is to demonstrate the radiation tolerant computer technology in a space environment under bombardment with statistically significant faults to verify reliable operation. The following figure shows the block diagram of the proposed satellite.
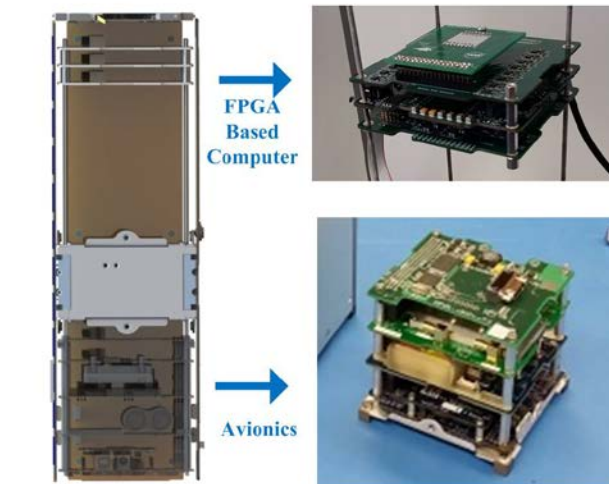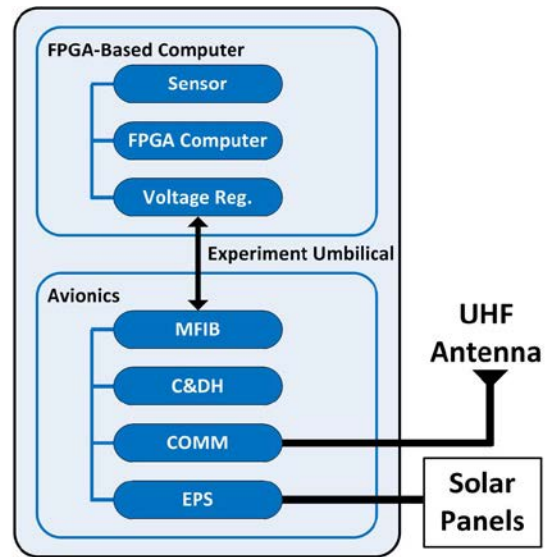

Figure 15: RadSat System Architecture.

The satellite contains two sub-systems, the avionics and the FPGA-based computer. The avionics sub-system contains the electrical power system (EPS), which interfaces with external solar panels to power the satellite. The EPS was designed and built at MSU in the SSEL. Also in the avionics is an Astronautical Development Helium 100 UHF/VHF radio, which serves as the communication link to the ground station located at MSU. The command and data handling system in the avionics is implemented using a Pumpkin CubeSat motherboard containing a PIC24 processor. The avionics system contains an interface board (MFIB) that is used to communicate and power other experiments within the satellite. An *Experiment Umbilical* is used to connect the avionics to an experiment and provides a single 9VDC voltage and a

bi-directional UART communication channel. The FPGA-based computer is architected as an experiment within the satellite. The FPGA system contains a local power regulation board, an FPGA board, and a radiation sensor board. It should be noted that the avionics sub-system has been flown on a prior CubeSat mission and the FPGA-based computer has been flown on a sounding rocket and has an upcoming demonstration on the International Space Station. The SSTP project has funded the integration of the two sub-systems into a full 3U CubeSat for an orbital demonstration of the computer technology.

Orbital Test Environment

The computer system technology has been matured as far as it can within a terrestrial environment. The next step in evaluating the SEE immunity of the computer is a flight demonstration in space. Space testing is required because the energy levels necessary to empirically test the system's SEE immunity cannot be produced on earth. Cyclotrons and particle accelerators cannot reproduce the space environment accurately and are typically used to bombard sub-systems in modified form factors such as exposed integrated circuits that have regions intentionally exposed to increase their SEE susceptibility. These types of tests do not meet the requirements of a full system prototype demonstration in an operational environment in order to achieve TRL-7. While high altitude balloons provide an easily accessible platform for flight testing, they do not reach a sufficiently high altitude to expose the computer system to the representative mission radiation environment nor do they provide sufficient time to perform a comprehensive evaluation of the system's reliability. Sounding rocket tests will enable the computer to reach a sufficient altitude (72 miles) to be exposed to the representative environment, but they also do not provide sufficient exposure time to perform a comprehensive analysis.

A high inclination, Low Earth Orbit that passes through the South Atlantic Anomaly and the poles is an ideal environment for demonstrating the computer's SEE mitigation strategy. This orbit provides a sufficient amount of time for the system to experience a reasonable number of faults to evaluate the system's radiation tolerance. Our team has extracted the predicted radiation strike and corresponding fault rates from the CRÈME96 tool if our system was flown on the ISS. The following figure shows a graphical depiction of the faults caused by heavy ions and those caused by trapped protons during a LEO orbit.
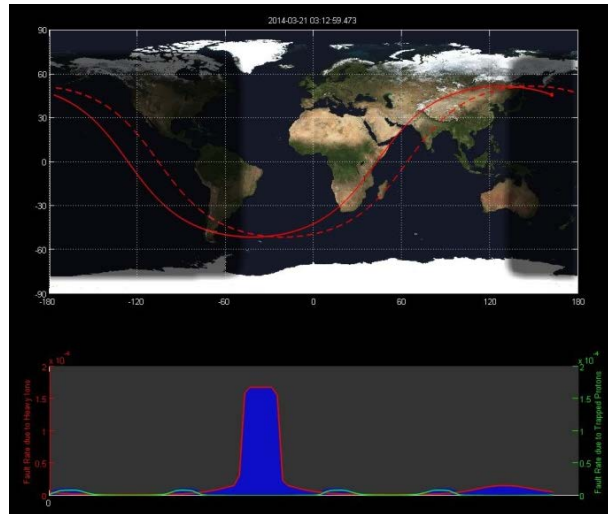

Figure 16: Anticipated Number of Faults in LEO for a Virtex-6 FPGA.

It is predicted that our system will experience 14 high energy radiation strikes per day, of which 2-3 will result in SEE faults. As anticipated, the largest number of faults occurs while passing through the south Atlantic anomaly and over the Earth's magnetic poles. The computer is expected to experience 2-3 faults per day, which results in ~2,000 faults during a 24 month orbit. This is a sufficiently large sample to verify the system's fault immunity. Our predictions correspond well to SEE data collected from the Goddard Space Flight Center's SpaceCube system (Virtex-4), which flew on the ISS as part of MISSE-7 [27]. The following figure shows the locations for SEEs experienced over the course of 10 months during ISS deployment. Our computer will experience approximately 20x more SEEs due to being fabricated in a more modern process node (Virtex-6 = 45nm vs. Virtex-4 = 90ns).

Figure 17: Location of SEEs during GSFC SpaceCube Deployment (Virtex-4) on MISSE-7 over 10 month Period [31].

The Next Steps

RadSat is currently being implemented and tested in a 3U form factor for environmental testing. RadSat has been accepted by the 2015 NASA CubeSat Launch Initiative (CSLI) program for a flight in 2016 or 2017. The ground operations for RadSat will be conducted at Montana State University, which currently has 5 CubeSats in orbit. The current work underway is finalizing the flight software and flight qualifying the unit. The following figure shows a rendering of the final RadSat satellite.
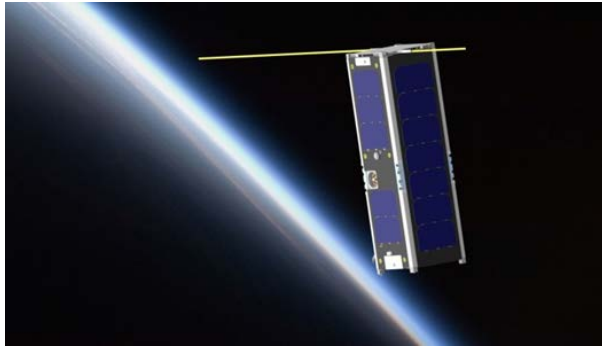

Figure 18: Rendering of Final 3U RadSat in LEO

Acknowledgments

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