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Pres #: 3.0101, Paper ID: 1080
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FPGA Implementation of a Bartlett Direction of Arrival Algorithm for a 5.8GHz Circular Antenna Array

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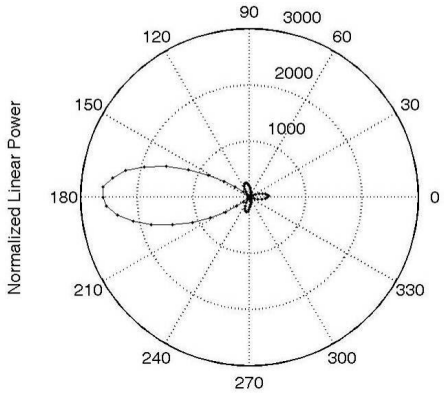
Presenter: Brock J. LaMeres

Motivation

Smart Antenna Systems

- **Directional radiation patterns used to:**

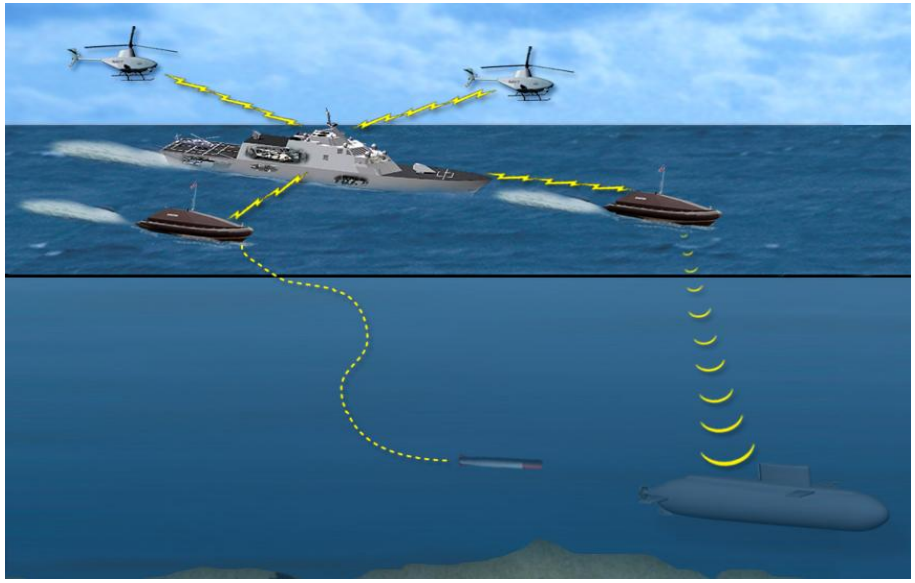
  - reduced transmit power
  - protect data from unwanted listeners
  - nullify interference



Directional Radiation Pattern

Courtesy Ericsson MW, Sweden

Secure Wireless Communication with Airborne Web Server

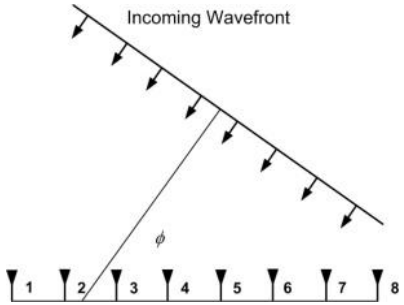


Integrated Multi-Platform Sonar System LCS Application

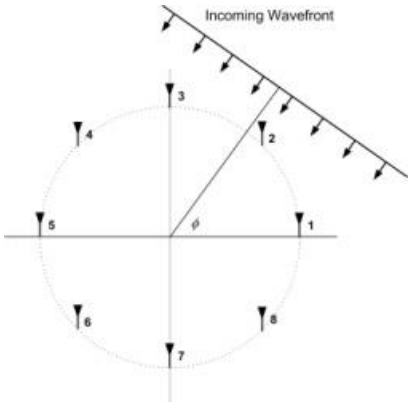
Motivation

Smart Antenna Components

1) Antenna Array

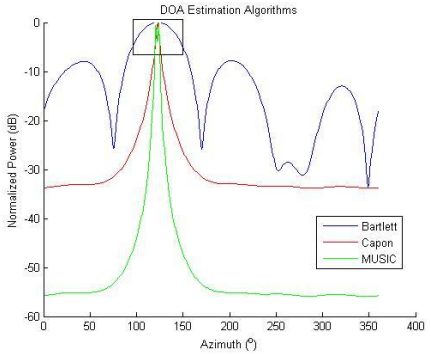


8-element uniform linear array



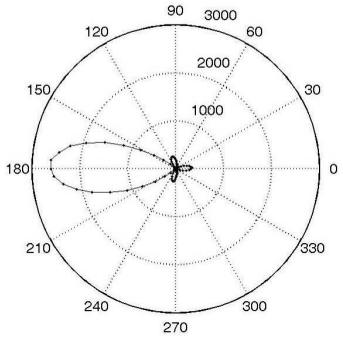
8-element uniform linear array

2) Direction-of-Arrival (DOA) Estimation (Rx)



Rx Power vs. Incident Angle

3) Beam Forming (Tx)



Directional Radiation Pattern

Motivation

Digital Beam Forming

- **Advantages over traditional analog systems**

  - Higher performance algorithms (MVDR, MUSIC)
  - Lower cost hardware
  - Integration allows lighter weight hardware
  - Frequency agility

- **Digital Implementation Options**

  - Custom Hardware (ASICs, VHDL-based FPGA design)
  - Microprocessors
  - Hybrid systems (custom & processor HW)

Our Work

Effective Digital Implementation of Direction-of-Arrival Estimation

- **Comparison of Implementation Techniques on FPGAs**

  - Custom Digital Hardware (VHDL)
  - Microprocessors System (Soft processor)
  - Hybrid (VHDL & Soft processor)

- **Performance Comparison of Subsystem Implementation**

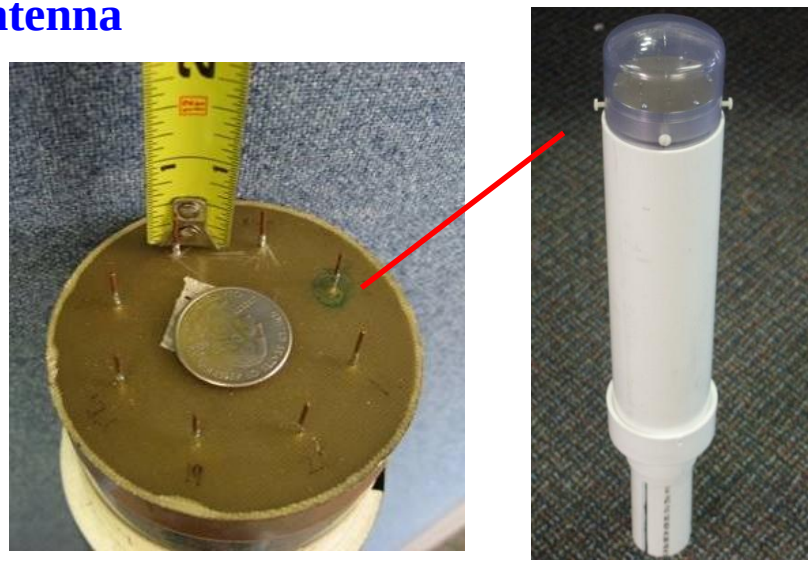
  - FFT
  - Frequency Detection
  - Bartlett Direction of Arrival Estimation

System Design

Subcomponents

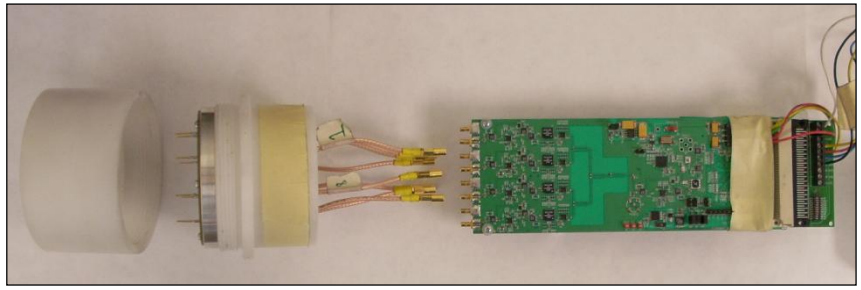
- **5.8 GHz, 8-element Circular Array Antenna**

  - Diameter = 76mm (3”)
  - Inter-element spacing
    = 0.37λ = 19mm (0.75”)



- **Receiver Board**

  - down conversion to IF
  - 5.8GHz to 10MHz



System Design

Subcomponents

- **8-Channel A/D Converter**

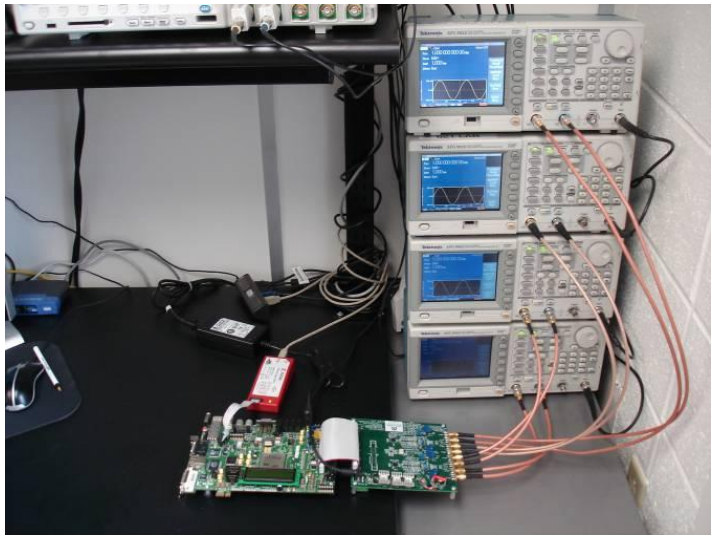
  - 2x 4-channel Analog Devices AD9287
  - 25 MSPS across all 8 channels

- **FPGA Processing Platform**

  - Xilinx Virtex-5 ML507 Eval Board
  - Virtex-5 FX70 FPGA

System Design

Test Setup

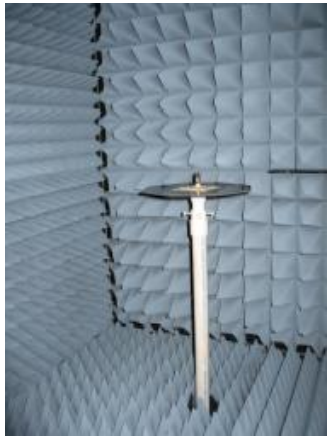


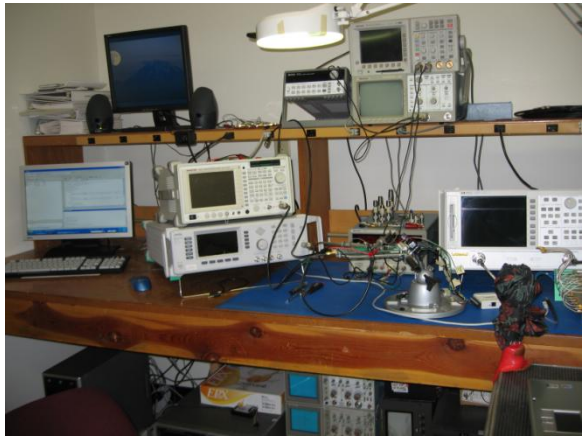
- **Phased IF Signal Generation**

  - drive emulated IF into ADC

- **Anechoic Chamber Testing**

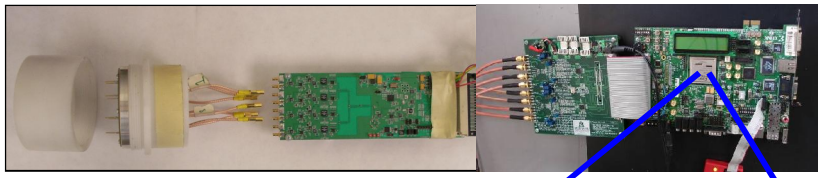
  -full receiver path



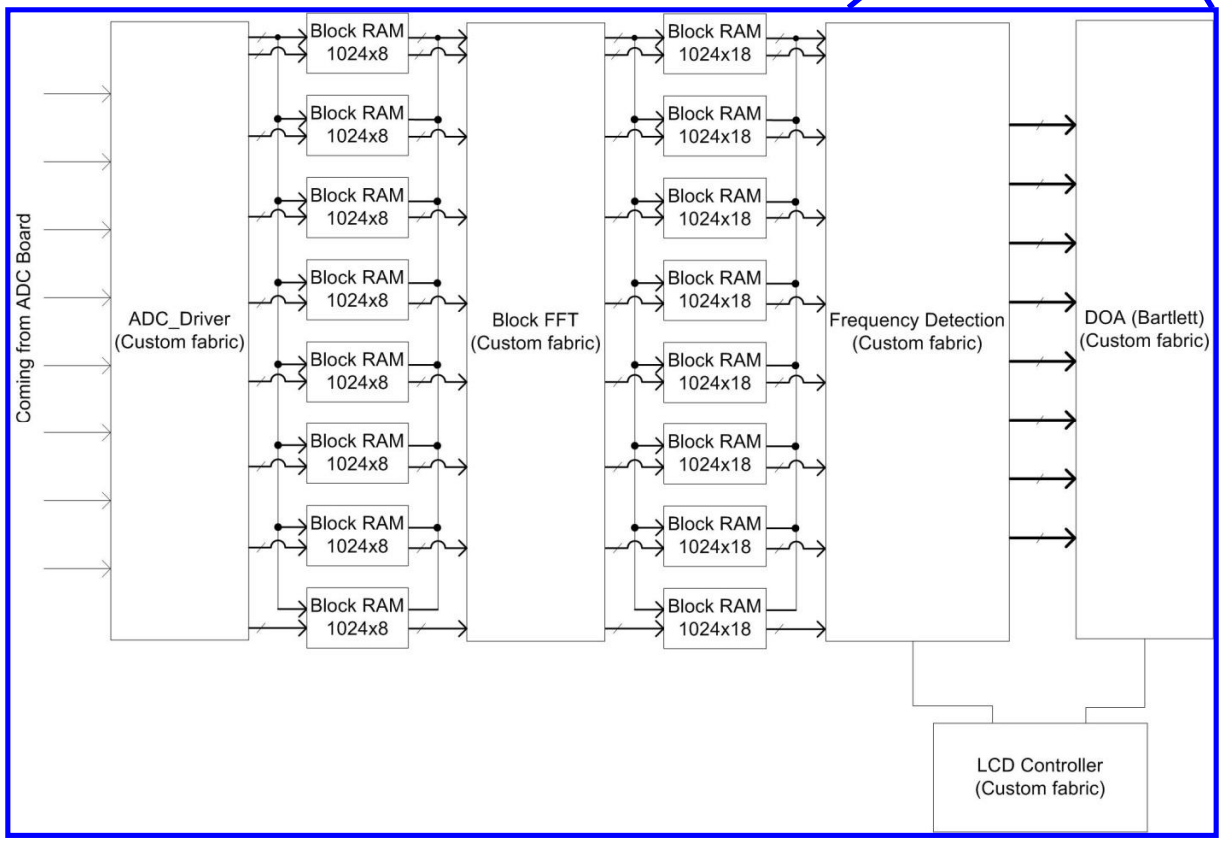


DOA Implementation (Custom Hardware)

Custom VHDL-Based FPGA Hardware

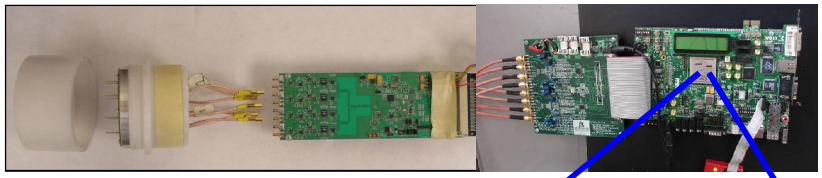


ADC Driver: Custom VHDL
Sample RAM: Xilinx Core
FFT: Xilinx Core
FFT RAM: Xilinx Core
Freq Detect: Custom VHDL
Bartlett DOA: Custom VHDL

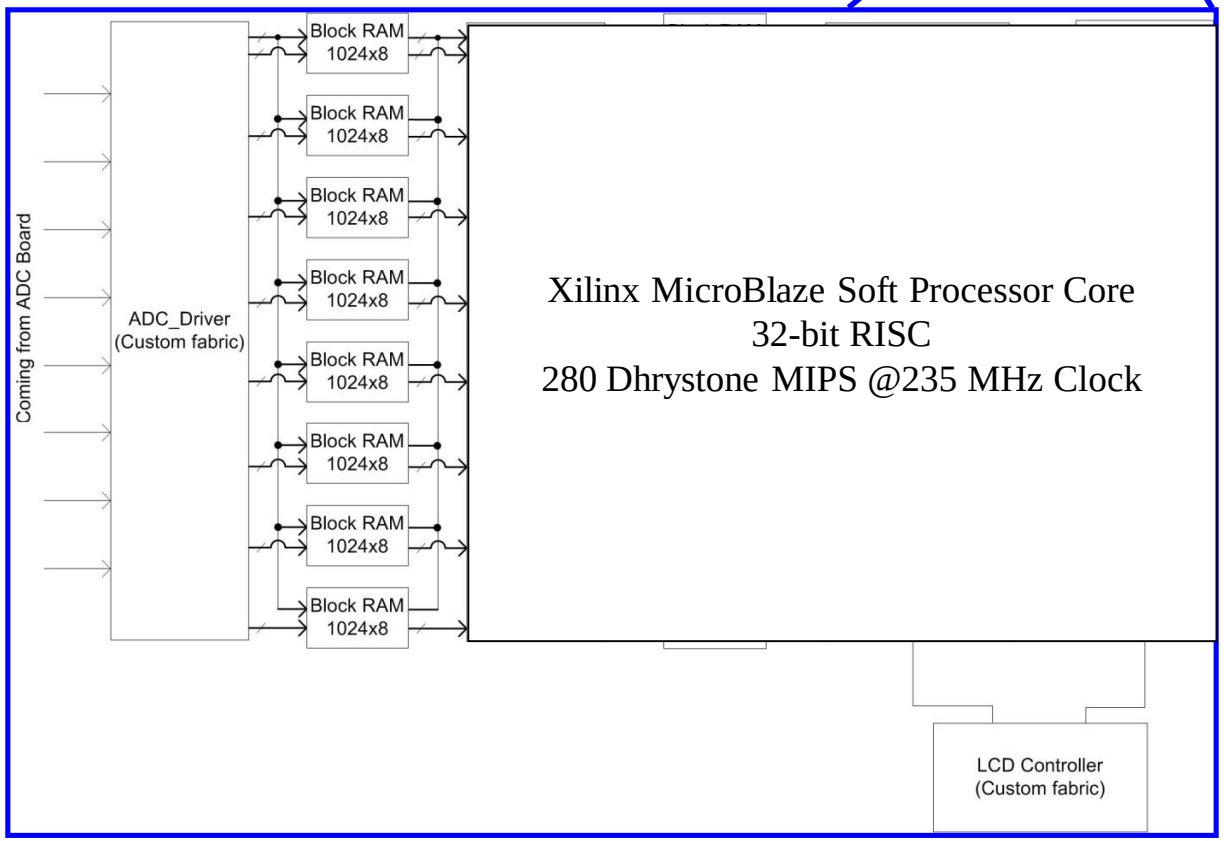


DOA Implementation (Microprocessor-based)

Microprocessor-Based FPGA Hardware



ADC Driver: Custom VHDL
Sample RAM: Xilinx Core
FFT: MicroBlaze
Freq Detect: MicroBlaze
Bartlett DOA: MicroBlaze



Performance Comparison

Hardware vs. Software

	Latency (µs)		Resources Estimation											
	HW	SW	Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
			HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

Computation Time by MicroBlaze Soft Processor
(summary for floating point FFT)

Computation Time by Custom VHDL

Performance Comparison

Hardware vs. Software (FFT)

Single Channel FFT – Fixed Point

	HW	SW	Comparison
Time	34.3 us	104,825 us	**HW is ~3000 times faster**
Area			**HW is 45% smaller**
- *Slices*	418	1494	
- *Registers*	1271	2172	
- *LUTS*	929	2349	
- *LUT RAM*	144	69	
- *DSP Slices*	9	5	
- *BRAM (18k)*	7	64	

	Latency (µs)		Resources Estimation											
	HW	SW	Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
			HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

Performance Comparison

Hardware vs. Software (FFT)

8-Channel FFT – Fixed Point

	HW	SW
Time	34.3 us	838,600 us
Area		
- *Slices*	3347	1494
- *Registers*	*10,172*	*2172*
- *LUTS*	*7434*	*2349*
- *LUT RAM*	*1147*	*69*
- *DSP Slices*	*72*	*5*
- *BRAM (18k)*	*20*	*64*

NOTE: MicroBlaze resources do not change once instantiated

Comparison

HW is ~24,500 times faster

SW is ~4 times smaller

	Latency (µs)		Resources Estimation											
	HW	SW	Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
			HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

Performance Comparison

Hardware vs. Software (Frequency Detection)

Fixed Point Frequency Detection

	HW	SW
Time	10.3 us	1007 us
Area		
- *Slices*	15	1494
- *Registers*	27	2172
- *LUTS*	18	2349
- *LUT RAM*	0	69
- *DSP Slices*	2	5
- *BRAM (18k)*	0	64

NOTE: MicroBlaze resources do not change once instantiated

Comparison

HW is ~100 times faster

HW is ~100 times smaller

	Latency (µs)		Resources Estimation											
	HW	SW	Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
			HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

Performance Comparison

Hardware vs. Software (DOA)

Bartlett Fixed Point DOA Estimation

	HW	SW
Time	1.73 us	310us
Area		
- *Slices*	58	1494
- *Registers*	*200*	*2172*
- *LUTS*	*165*	*2349*
- *LUT RAM*	*0*	*69*
- *DSP Slices*	*0*	*5*
- *BRAM (18k)*	*0*	*64*

NOTE: MicroBlaze resources do not change once instantiated

Comparison

HW is ~180 times faster

HW is ~8 times smaller

	Latency (µs)		Resources Estimation											
	HW	SW	Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
			HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

Performance Comparison

Hardware vs. Software (Complete Computation)

Fixed Point DOA Computation

	HW	SW
Time	46 us	839,917 us
Area		
- *Slices*	3420	1494
- *Registers*	*10399*	*2172*
- *LUTS*	*7617*	*2349*
- *LUT RAM*	*1147*	*69*
- *DSP Slices*	*74*	*5*
- *BRAM (18k)*	*20*	*64*

NOTE: MicroBlaze resources do not change once instantiated

Comparison

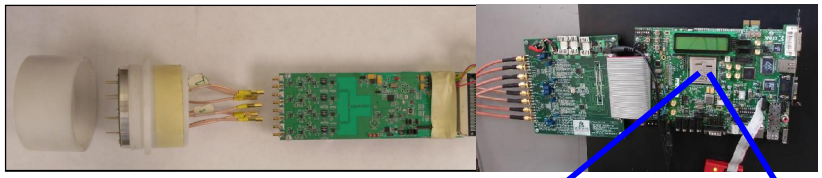
HW is ~18,000 times faster

SW is ~4 times smaller

	Latency (µs)		Resources Estimation											
			Slices		Slice Register		LUTs		LUTRAM		XtremeDSP Slices		18K Block Ram	
	HW	SW	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC	HW	SC
FFT														
Fixed Pt														
- Serial	274.5	838600	NA		NA		NA		NA		9		7	
- Parallel	34.31	104825	3347		10172		7434		1147		72		20	
Floating Pt														
- Serial	357.84	608,800	NA		NA		NA		NA		24		18	
- Parallel**	44.73	75880	NA		NA		NA		NA		192		144	
Freq Det														
- Fixed Pt	10.3	1007	15		27		18		0		2		0	
- Floating Pt	NA	751	NA		NA		NA		NA		NA		NA	
Bartlett														
- Fixed Pt	1.73	310.4	58		200		165		0		0		0	
- Floating Pt	NA	244.4	NA		NA		NA		NA		NA		NA	
MicroBlaze		684,000		1494		2172		2349		69		5		64

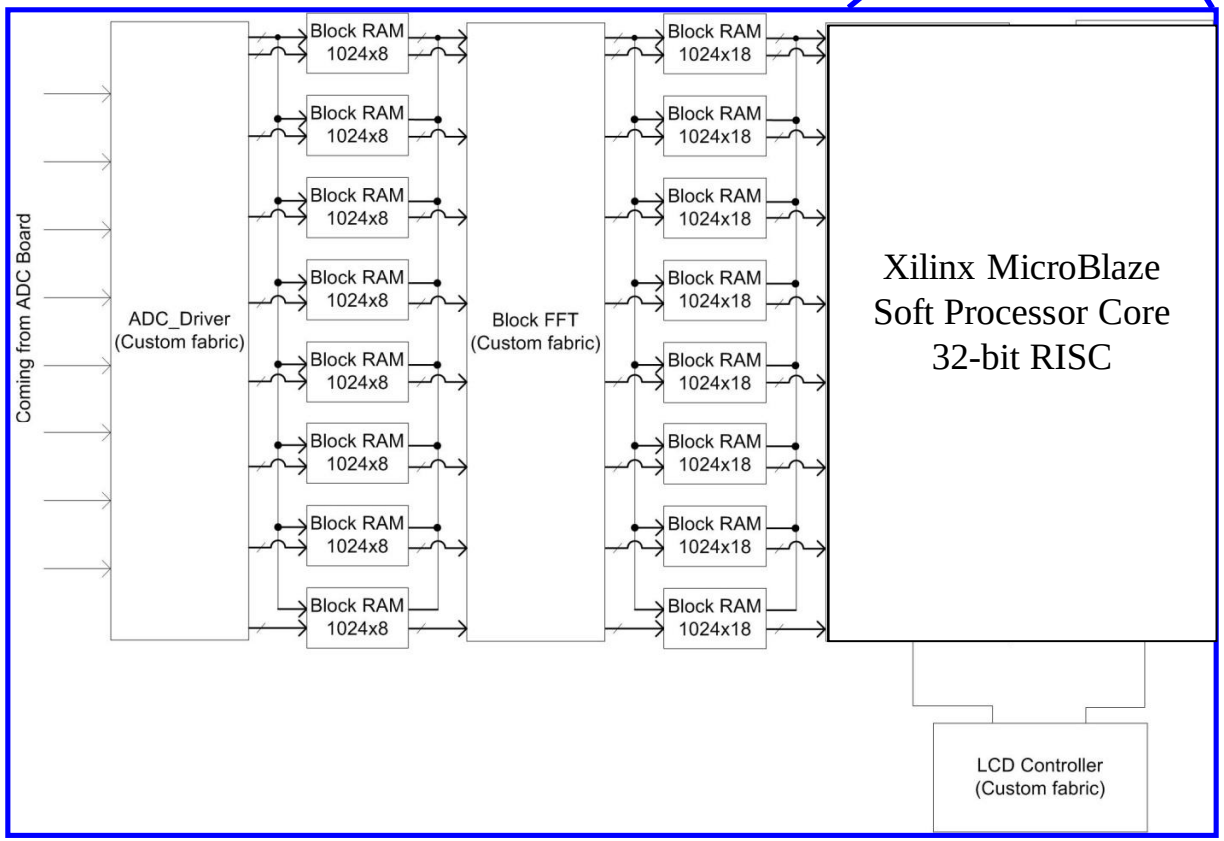
DOA Implementation (Hybrid)

Custom VHDL + Microprocessor FPGA Hardware



Largest Computation Time = FFT (move to HW)

ADC Driver: Custom VHDL
Sample RAM: Xilinx Core
FFT: Xilinx Core
FFT RAM: Xilinx Core
Freq Detect: MicroBlaze
Bartlett DOA: MicroBlaze



Performance Comparison

Hardware vs. Software (Complete Computation)

Fixed Point DOA Computation

	HW	SW	Hybrid	Comparison
Time	46 us	839,917 us	1351 us	**Hybrid is ~30x slower than HW** **Hybrid is ~620x faster than SW**
Area				
- *Slices*	3420	1494	4841	
- *Registers*	*10399*	*2172*	*12,978*	
- *LUTS*	*7617*	*2349*	*9783*	**Hybrid is ~1.5x larger than HW**
- *LUT RAM*	*1147*	*69*	*1216*	**Hybrid is ~5x larger than SW**
- *DSP Slices*	*74*	*5*	*79*	
- *BRAM (18k)*	*20*	*64*	*84*	

Why a Hybrid?

1) Development Time (Cores + Processor = Fastest Development Time)
2) Back-end Flexibility (Basic IO, Post Processing)

Summary

Overview

- A Bartlett DOA Estimation was implemented on an FPGA using a variety of techniques

    - VHDL-based Hardware
    - Xilinx IP Cores
    - Soft processors
    - Hardware
    - Fixed vs. floating point computation

- Custom hardware provides increased performance

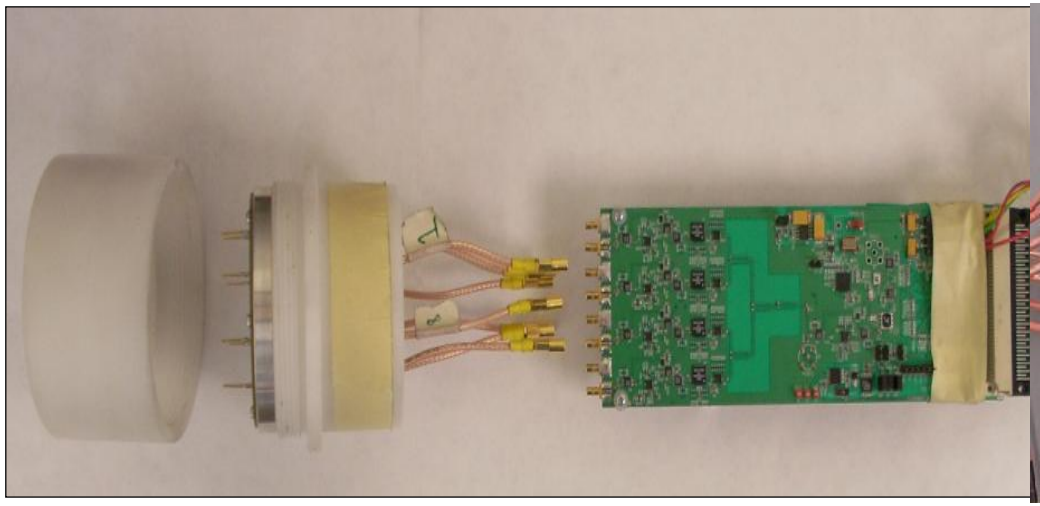
- Software provides fixed resource allocation

- A Hybrid approach minimizes critical path circuitry

- Development time dominates custom HW development

- Xilinx IP cores alleviate some development time issues with custom HW

Questions



MONTANA STATE UNIVERSITY

ADVANCED ACOUSTIC CONCEPTS