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Mountains & Minds

# Controlled Impedance Chip-to-Chip Interconnect Using Coplanar Wire Bond Structures

MSGC
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Sam Harkness, Jeff Meirhofer, & Brock J. LaMeres
Electrical & Computer Engineering Dept.
Montana State University
Bozeman, MT 59717

## Introduction

### 3D PACKAGING

- Integration Multiple Dies within a single package:
  - Allows optimization of substrate materials for application.
  - Mitigates power density issues from high transistor counts.
  - Allows economical design partitioning.
- Improved electrical performance:
  - Replaces package PCB traces with shorter wire bonds.

### WIRE BONDS

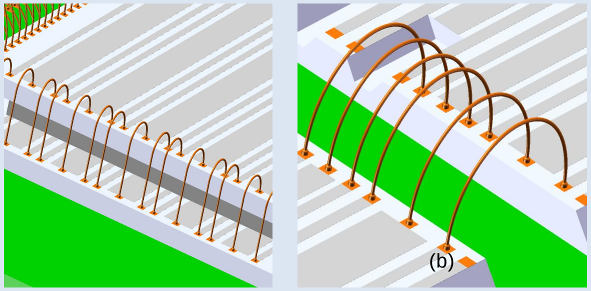
- Most common interconnect due to flexibility and low cost.
- Historically has not had to be treated as distributed element due to its relative length compared to system level T-lines

### PROBLEM STATEMENT

- Today, CMOS edge rates are now fast enough to force wire bonds to behave as distributed elements.
- Distributed noise sources such as reflections due to impedance discontinuities need to be considered.

## Proposed Solution

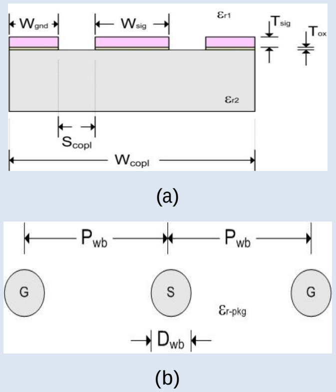
- Create controlled impedance T-lines for chip-to-chip signaling using 3-wire coplanar structures.
- On-chip: G-S-G coplanar wire bonds.
- Off-chip: G-S-G coplanar T-lines.



(a)

Fig 1. 3-D Rendering of our interconnect approach used in System-in-Package application with (a) adjacently-placed dies and (b) stacked-dies. Coplanar transmission lines on the two dies are connected using a G-S-G wire bond configuration.

## System Design



(b)

Fig 2. Critical dimensions for the (a) on-chip coplanar traces and the (b) off-chip coplanar wire bond structures.

### PARAMETERS

- Wire Bond
  - $D_{wb}$: Wire Diameter
  - $P_{wb}$: Wire Pitch
  - $\varepsilon_{r,\,pkg}$: Encapsulate Permittivity
- On Chip
  - Design Variables
    - $W_{gnd}$: Width of GND Trace
    - $W_{sig}$: Width of SIG Trace
    - $S_{copl}$: Space between GND & SIG
    - $W_{copl}$: Width of Coplanar Structure
  - Fabrication Constants
    - $T_{sig}$: Thickness of Metal Layer
    - $T_{ox}$: Thickness of Insulator
    - $\varepsilon_{r1}$: Permittivity of Encapsulate
    - $\varepsilon_{r2}$: Permittivity of Substrate

### CASE STUDY

- 50Ω and 75Ω terminated systems
- Gold wire and Aluminum wire
- 25 μm, 50 μm, and 75 μm wire

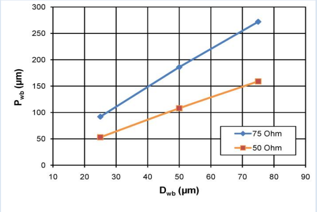


Fig 3. Pitch vs. Diameter for the controlled impedance coplanar wire bond structure showing both a 50Ω and 75Ω system.

| Structure | Param | Units | Dimensions | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 50 Ω | | | 75 Ω | | |
| Wire Bond<br>($\varepsilon_{r\text{-}pkg}$=4.3) | $D_{wb}$ | μm | 25 | 50 | 75 | 25 | 50 | 75 |
| | $P_{wb}$ | μm | 53 | 108 | 159 | 92 | 186 | 272 |
| Coplanar<br>($\varepsilon_{r1}$=4.3)<br>($\varepsilon_{r2}$=11.7) | $T_{sig}$ | μm | 1 | 1 | 1 | 1 | 1 | 1 |
| | $T_{ox}$ | μm | 1 | 1 | 1 | 1 | 1 | 1 |
| | $W_{sig}$ | μm | 26 | 48 | 74 | 24 | 44 | 76 |
| | $W_{gnd}$ | μm | 50 | 100 | 150 | 50 | 100 | 150 |
| | $S_{copl}$ | μm | 30 | 68 | 94 | 110 | 228 | 318 |

Table I. Dimensions for the matched impedance interconnect system for three sizes of commercially available wire bonds.

## Finite Element Analysis

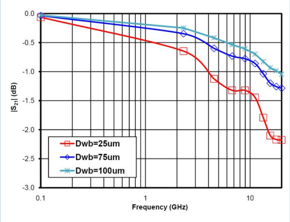


Fig 4. $|S_{21}|$ response for the 50Ω system with Aluminum wire bonds

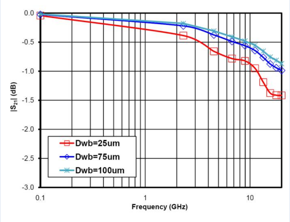


Fig 5. $|S_{21}|$ response for the 75Ω system with Aluminum wire bonds

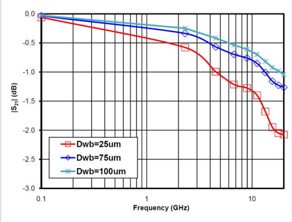


Fig 6. $|S_{21}|$ response for the 50Ω system with Gold wire bonds

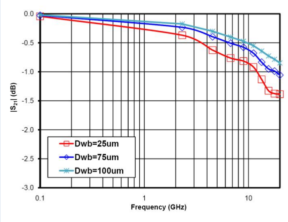


Fig 7. $|S_{21}|$ response for the 75Ω system with Gold wire bonds

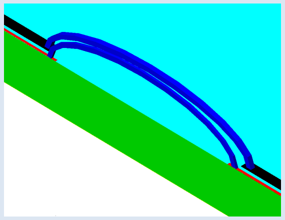


Fig 8. Interconnect structure used for Finite Element Analysis (FEA).

- In all cases, the loss of the system remains above -2.2dB up to 20GHz.
- The 75Ω systems outperform the 50Ω systems due to the inherent advantage of lower attenuation in higher impedance systems.
- The Gold wires outperform the Aluminum wires due to the increased conductivity of the metals