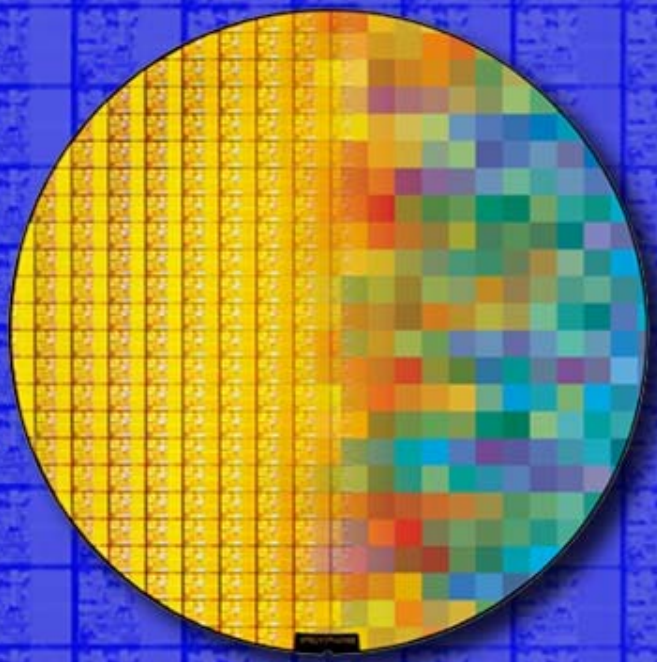
Challenges In Debugging At 5GHz



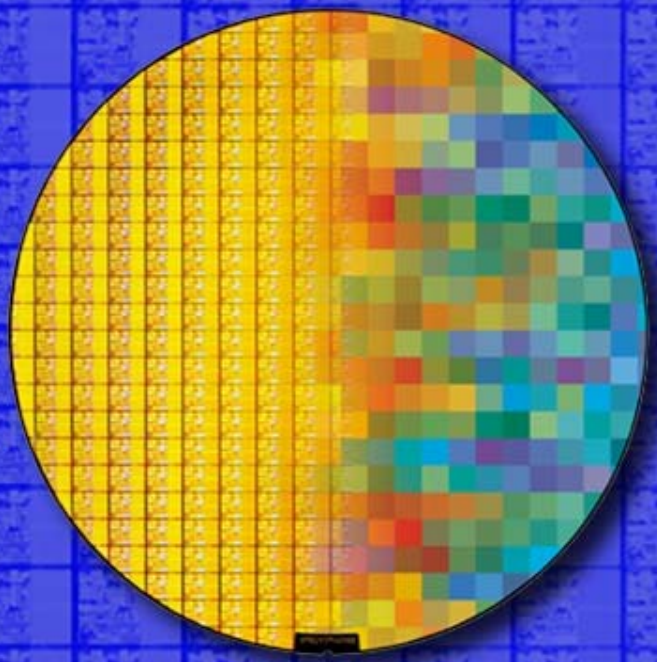
Fall IDF 2005
Session PCIS011

Host: Robert Vezina
Intel Industry Enabling

Presenters: Brock LaMeres
Agilent Technologies

John Calvin
Sarah Boen
Tektronix, Incorporated

Intel Developer FORUM



Gen 2 Probing Concerns and Best Practices

Brock J. LaMeres
HW Design Engineer
Agilent Technologies

Agilent Technologies

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Agenda

- Challenges of operating above 2.5Gb/s
- Theory of snoop probing
- Challenges of probing above 2.5Gb/s
- Probing solutions

Challenges of Operating above 2.5Gb/s

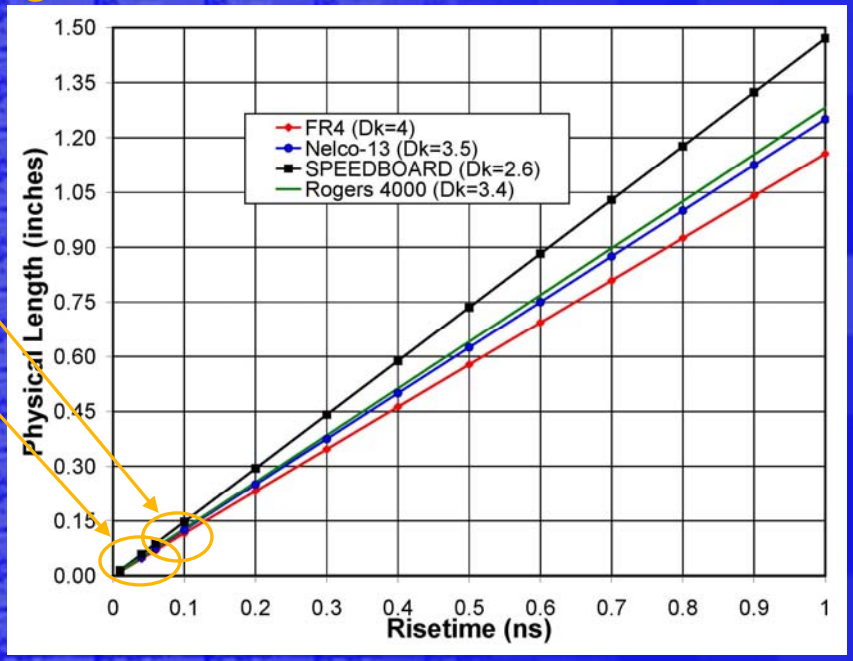
Shrinking Transmission Line Geometries

- Once negligible geometries must now be considered distributed.
- Almost everything in the system effects performance.

"Length that Structures Become Distributed"

PCI Express* Gen 1

PCI Express Gen 2



Less than 0.1" must be treated as distributed element

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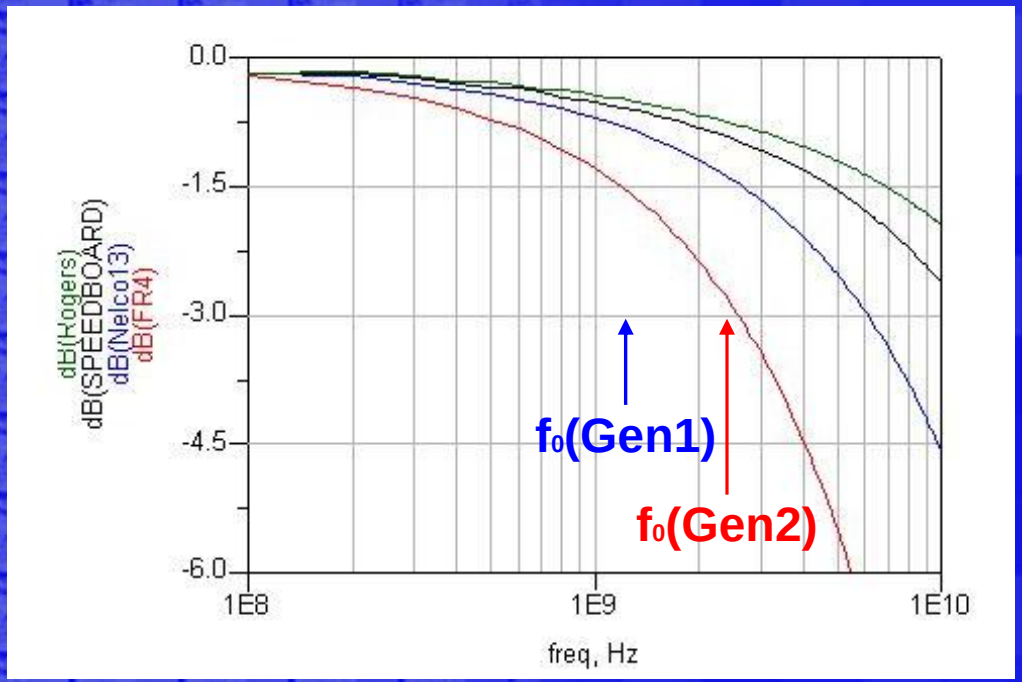
Challenges of Operating above 2.5Gb/s

Material Breakdown

- Dielectric loss and skin effect roll-off the signal and shrink the eye
- Advanced materials are often cost-prohibitive for large scale volumes

"Dielectric Loss of 10" of PCB Trace"



Cost

Performance

Low-Cost Dielectrics roll-off the signal

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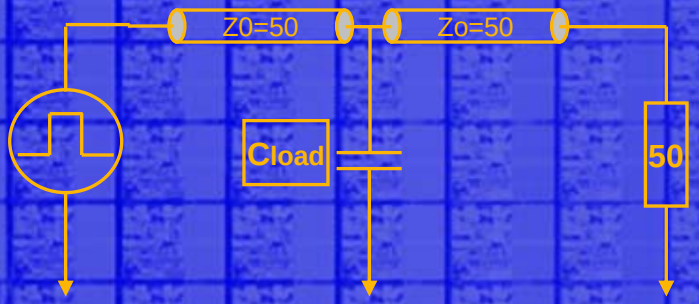
Challenges of Operating above 2.5Gb/s

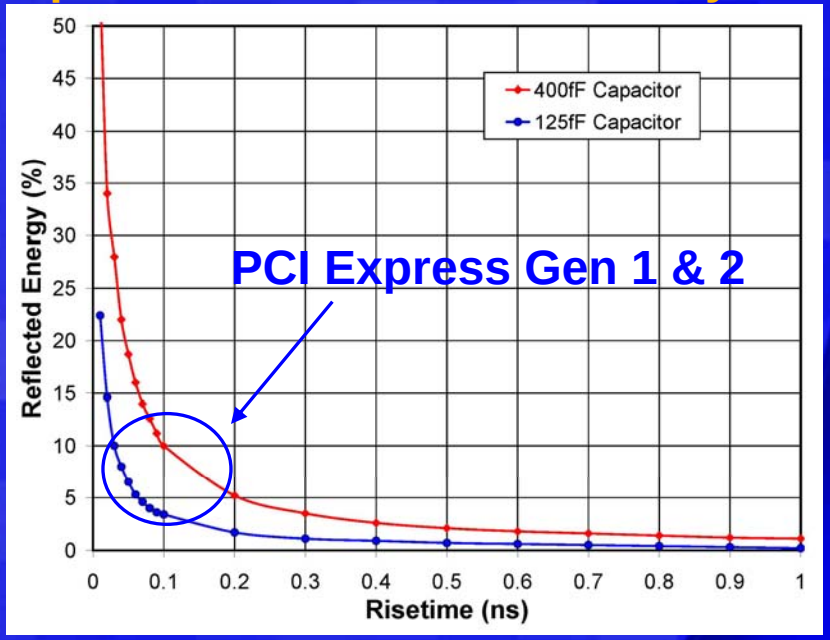
Reflections and ISI

- Un-matched impedances cause noise which shrinks eye.
- Impossible to avoid features required by manufacturability.



Faster Risetimes = More Reflected Energy

"Capacitive Reflections in 50Ω System"



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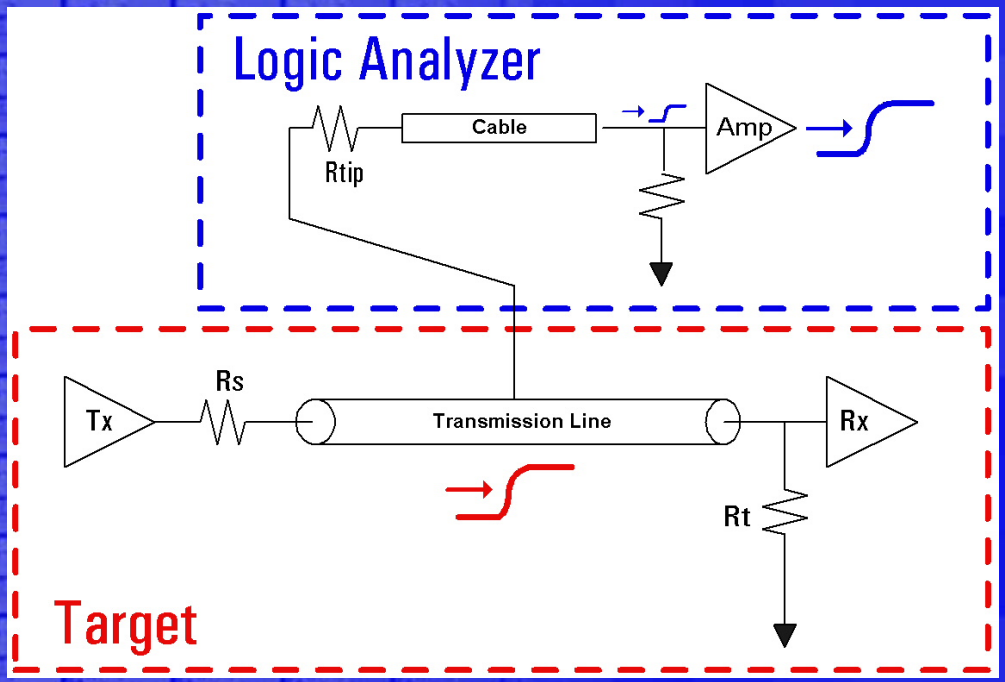
Snoop Probing Theory

Resistive Divider Architecture

- The probe takes a small part of the signal
- The target eye is reduced, the probed eye is small to begin with



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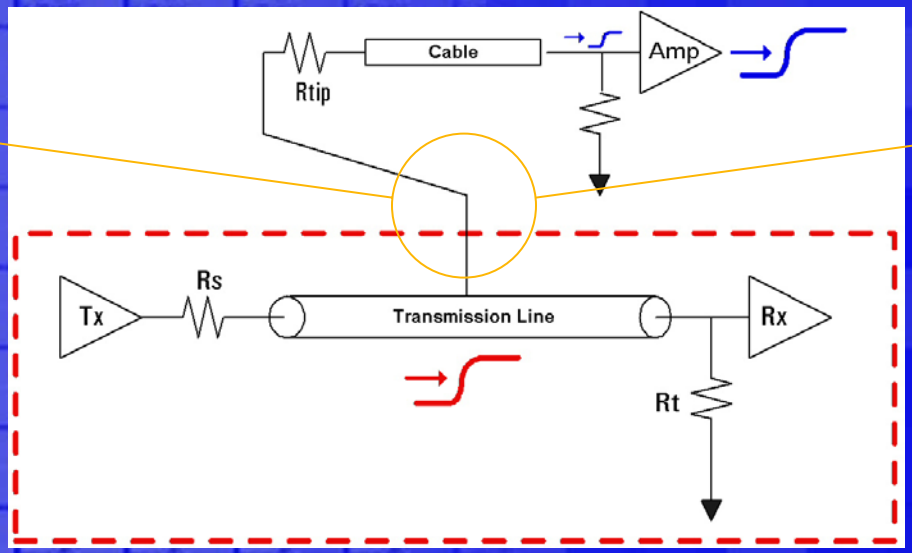
Snoop Probing Theory

Physical Interconnect Causes Loading

- The stub between the probe tip and target causes AC load.
- This stub is dictated by the physical interconnect structure

Interconnect
- PCB Trace
- Wires
- Connectors
- Springs



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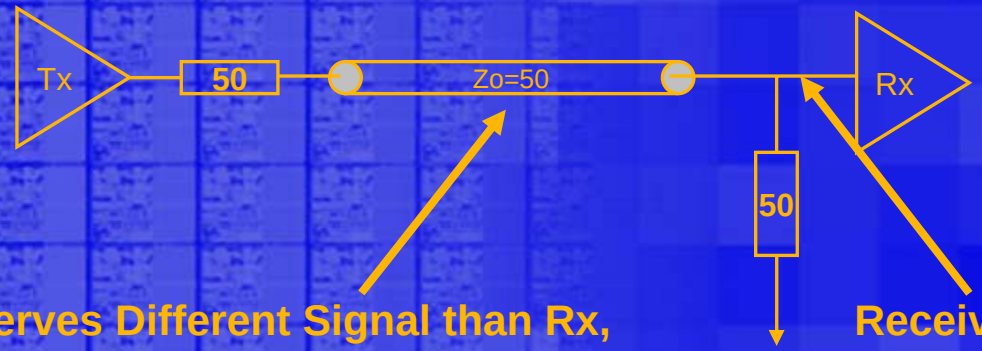
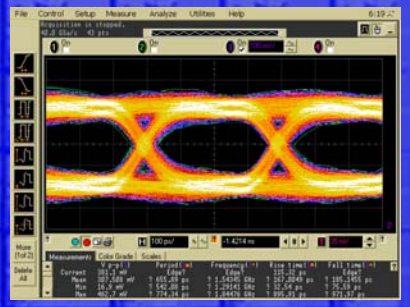
Snoop Probing Theory

Minimum Eye Must Exist at the Probe Tip

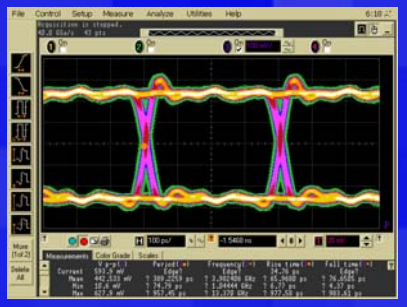
- Probe must have enough eye at the tip to acquire data successfully
- Bus specs are only valid for the waveform at the Rx



Probe Observes Different Signal than Rx, typically with less signal integrity



Receiver Observes Signal with Best Signal Integrity



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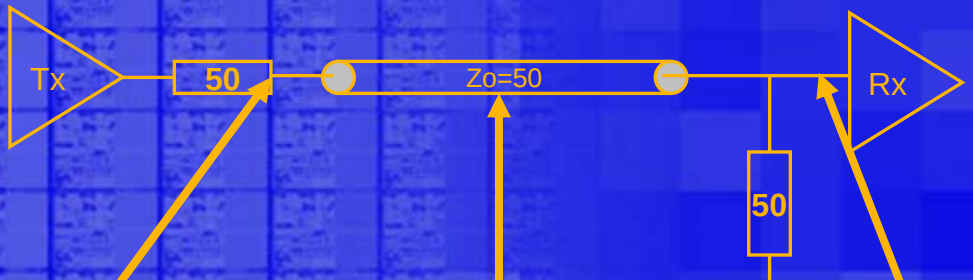
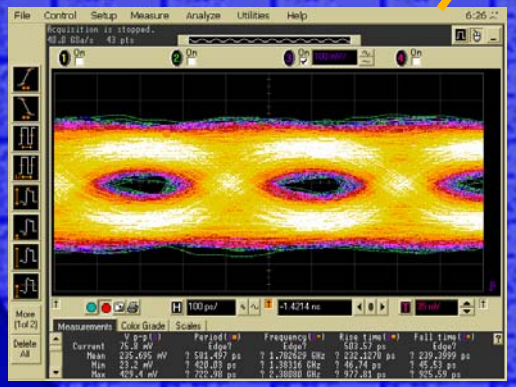
Challenges of Probing Above 2.5Gb/s

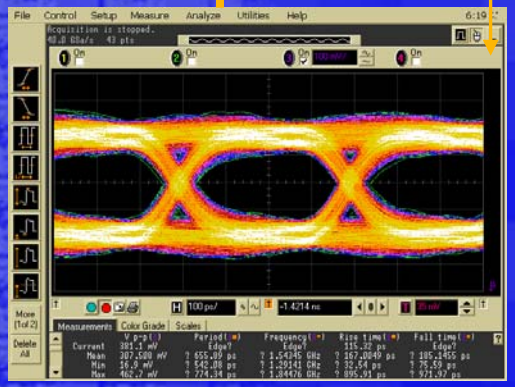
Probe Not Located Directly at Rx

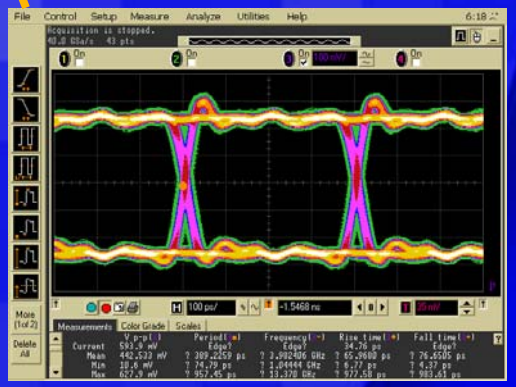
- Probe observes different signal than the Rx.
- Eye at the probe can be smaller due to reflections, ISI, and Dk loss
- Eye at the probe can be distorted due to pre/post emphasis.

Signal Quality degrades as you move away from Rx









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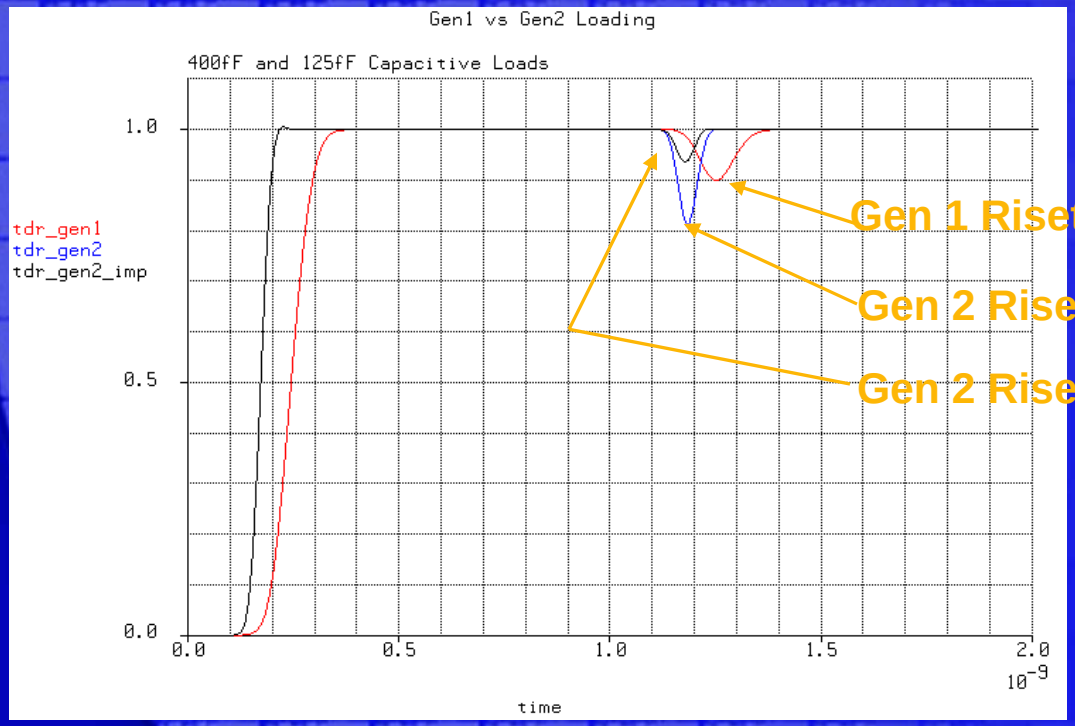
Challenges of Probing Above 2.5Gb/s

Reduced Probe Loading is Critical

- Tip network must be closer to target requiring advanced interconnect
- Interconnect reliability is a concern for electrically superior interconnect



Gen 1 Risetime (100ps), 400fF Probe Load = 10%

Gen 2 Risetime (50ps), 400fF Probe Load = 20%

Gen 2 Risetime (50ps), 125fF Probe Load = 2.5%

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Probing Solutions for Above 2.5Gb/s

Gen 1 Solutions (≤2.5Gb/s)

Midbus Probe

- Footprint placed on target
- Signals passively observed

Slot Interposer Probe

- Probe inserted between card and system
- Signals passively observed

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Probing Solutions for Above 2.5Gb/s

Gen 2 Solutions (2.5Gb/s - 5.0Gb/s)

Midbus Probe

- Able to passively observe at 5Gb/s

Slot Interposer Probe

- signal integrity issues from connector decreases eye.
- Safest Option : use Midbus probe

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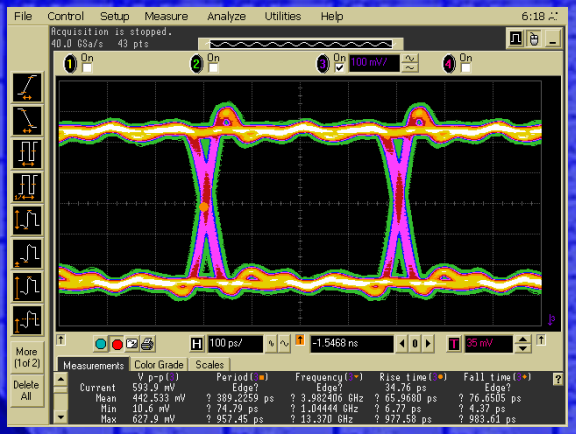
Summary

- **Achieving 5Gb/s for Gen 2 is a complex Signal Integrity Problem**
  - **Reflections, Dk Loss, Skin Effect, ISI.**
- **Probing at 5Gb/s is also an SI Problem**
  - Eye shrinkage at probe tip, reflections, ISI.
- **Successful Debug Requires Consideration of the System *and* Probe**



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Tektronix Testing Considerations for Gen2 PCI Express*

John Calvin
Solutions Engineering, Performance Oscilloscopes
Sarah Boen
Computer Segment Marketing, Logic Analyzers

August 2005

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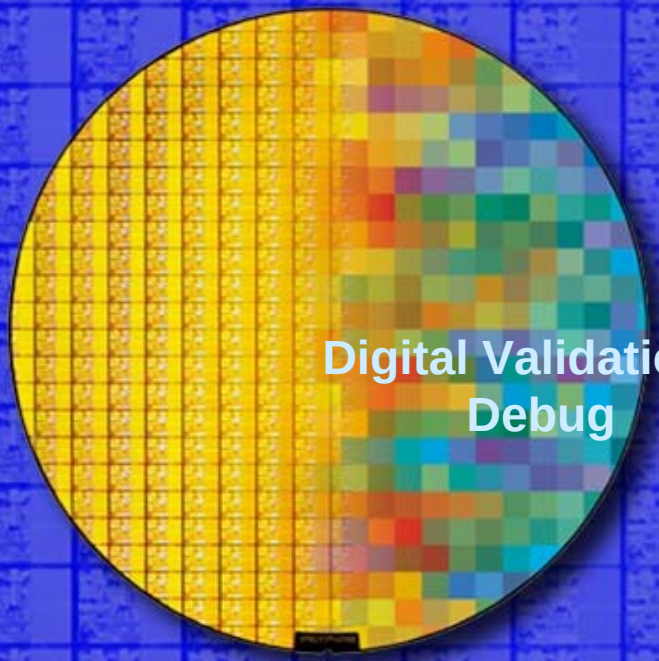
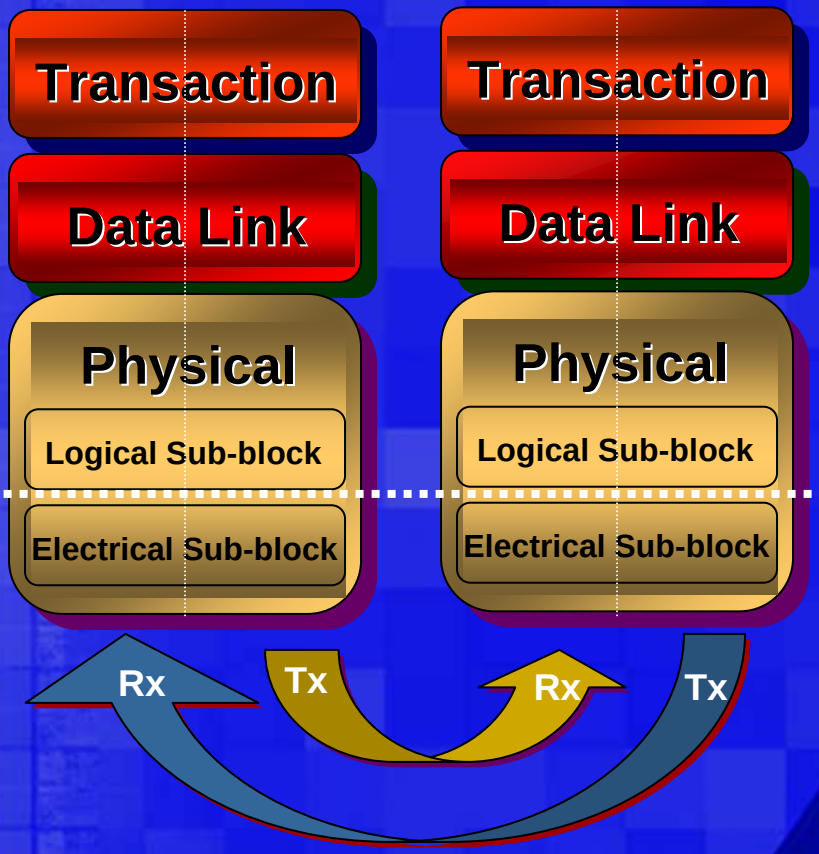
Analog Validation and Compliance



Analog Validation & Compliance



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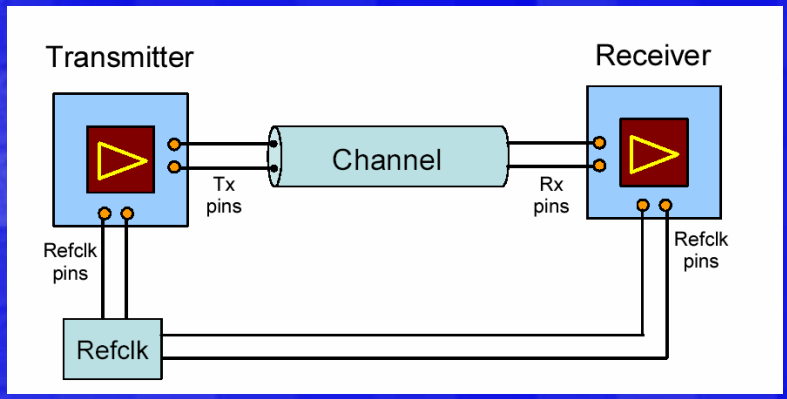
Electrical Sub block and Test Points

- Serial Data Test Points
  - Transmitter
  - Channel Interconnect
    - Card-Card
    - Card-Cable
  - Receiver



- Reference Clock Test Point
- 5Gb/s Specified in Section 4 of Base Spec
  - Gen2 link must meet Gen1/Gen2 specs for speed switching
- Recommended Tutorial
  - http://www.pcisig.com/members/downloads/events/devcon05/presentations/PCIe_20_Electrical_Parameters_Tutorial.pdf

Electrical Parameters

- Carried Forward
  - Eye Diagrams
    - Tbit, NTbit separation
  - Amplitude Timing Measurements
- New in Gen2
  - Evolution to Dual-Dirac Jitter (Tj-dd, Dj-dd)
  - De-convolution of Channel Model
  - Reference clock compliance
    - Removal of Ref Clk jitter from system jitter budgets.
  - Receiver testing
    - Tolerance testing.

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Evolution of CDR and Jitter Testing

- Rev1.0a
  - 3500:250 Window Clock Recovery
  - Median-Max-Outlier Jitter over any 250
- Rev1.1
  - 1st Order PLL for Clean Clock
  - Jitter measured over 1Million UI
  - 3500:250 still used for Dirty or SSC
  - Jitter @ 10-12 BER added to CEM Spec
  - Reference: http://www.pcisig.com/specifications/pciexpress/technical_library/PCIe_Rj_Dj_BER_R1_0.pdf
- Gen2 (Rev0.5)
  - PLL Filter Mask
    - 1st or 2nd Order function
  - Dual-Dirac Jitter
  - TJ-DD and DJ-DD @ 10-12 BER

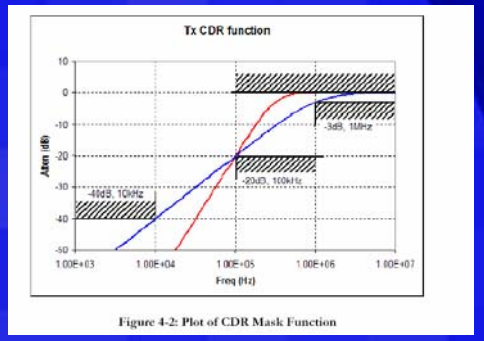
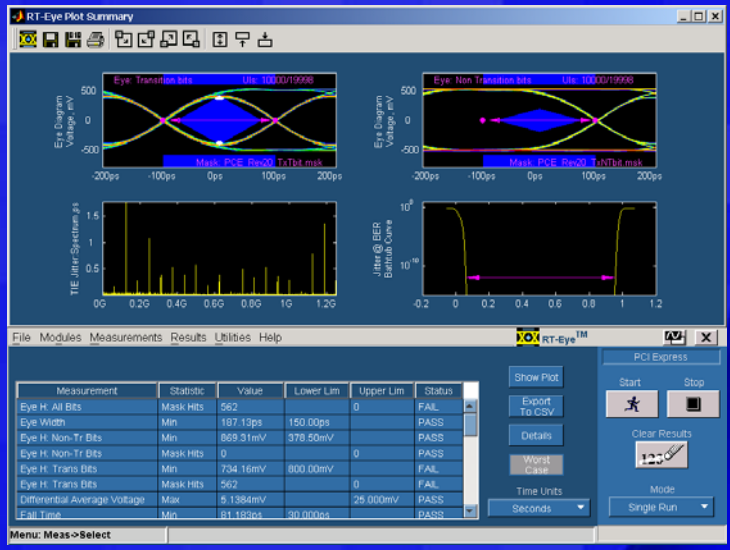


Figure 4-2: Plot of CDR Mask Function



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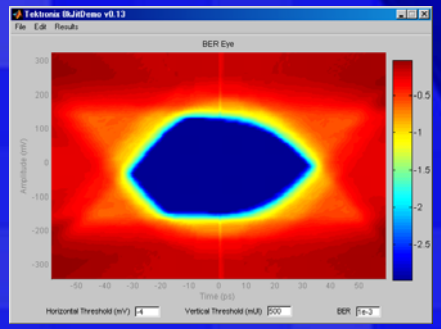
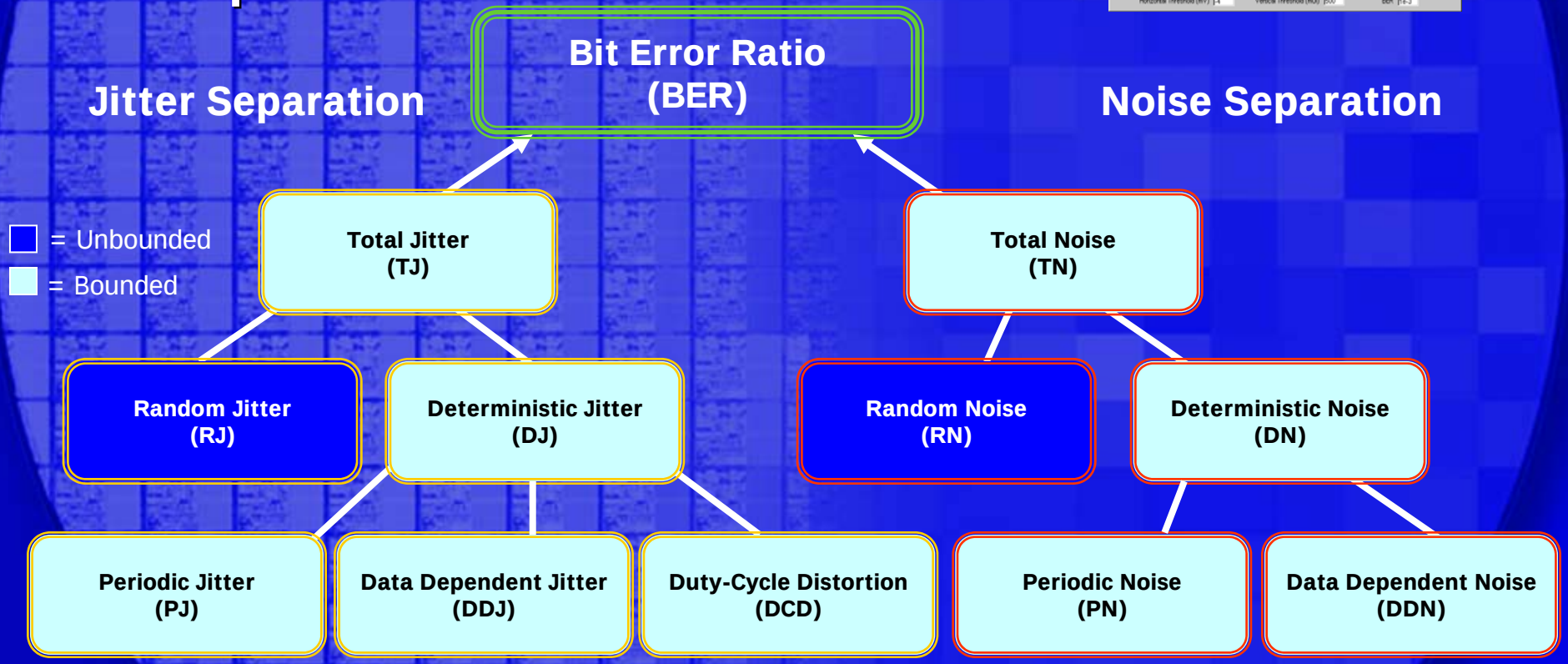
The evolution continues...

for More Accurate BER Analysis

- New Sampling (ET) Sampling Scope technique





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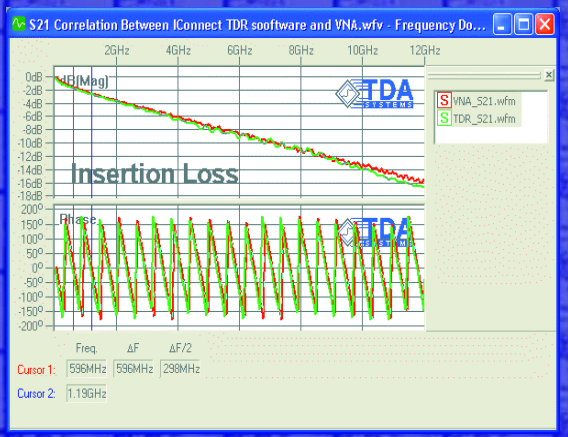
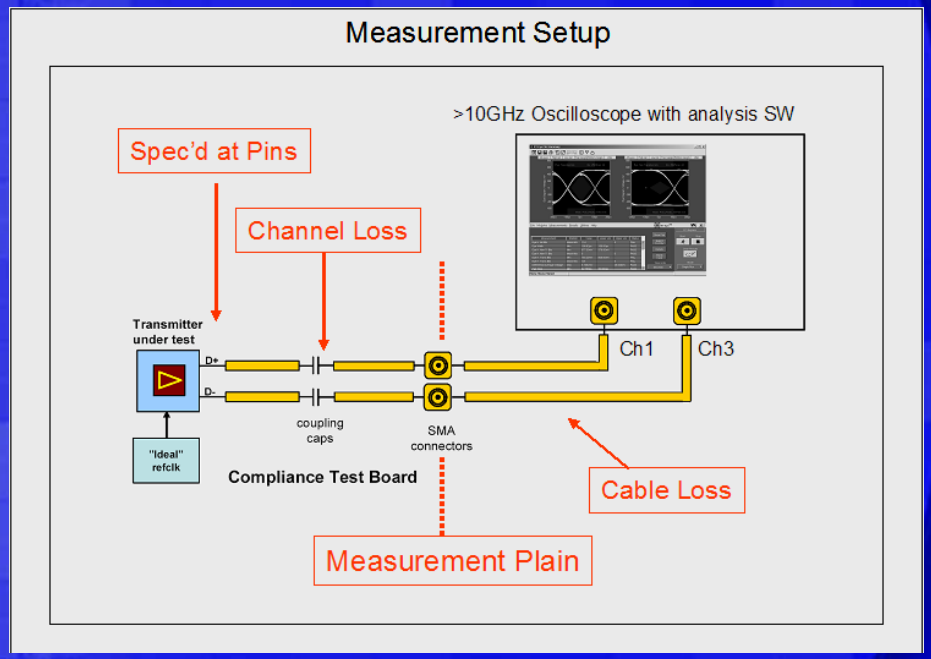
De-convolution of channel parameters

- Channel and Cable Loss
  - Characterize using or TDNA
- Analysis
  - Requires pre-filtering
  - Amplitude & Phase





1. Measurements require an oscilloscope with a bandwidth of at least 10 GHz. Measurement must deconvolve effects of compliance test board to yield an effective measurement at Tx pins. At least 10^6 samples must be acquired.

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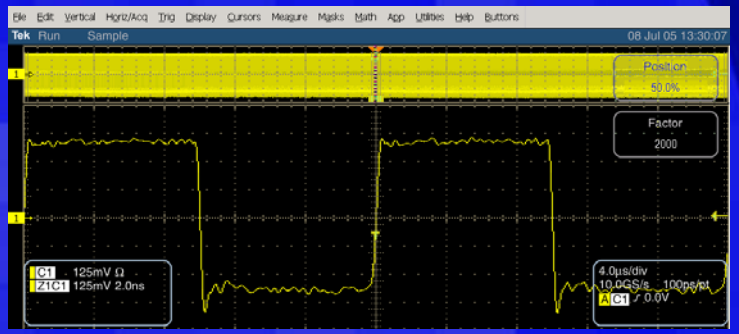
RefClk Compliance Measurements

- **Reference Clock Compliance Test**
  - Acquire Differential RefClk
  - Filter Using Jitter Mask Function
  - Analyze Jitter
  - Analyze other Parameters
  - Apply Spec limits
  - Report Pass/Fail Results

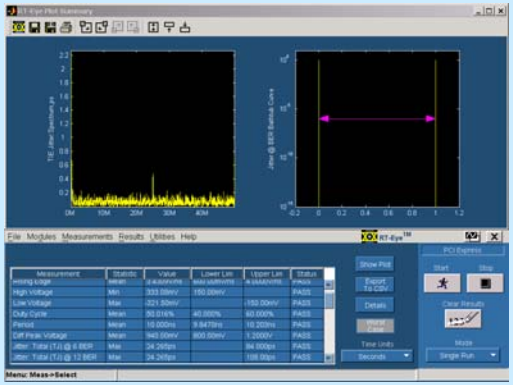


Differential RefClk

Jitter Mask Function

$$H_1(s)=\left[\frac{2s\zeta_2\omega_{n2}+\omega_{n2}^2}{s^2+2s\zeta_2\omega_{n2}+\omega_{n2}^2}e^{-sT_1}-\frac{2s\zeta_1\omega_{n1}+\omega_{n1}^2}{s^2+2s\zeta_1\omega_{n1}+\omega_{n1}^2}\right]$$

Results Display



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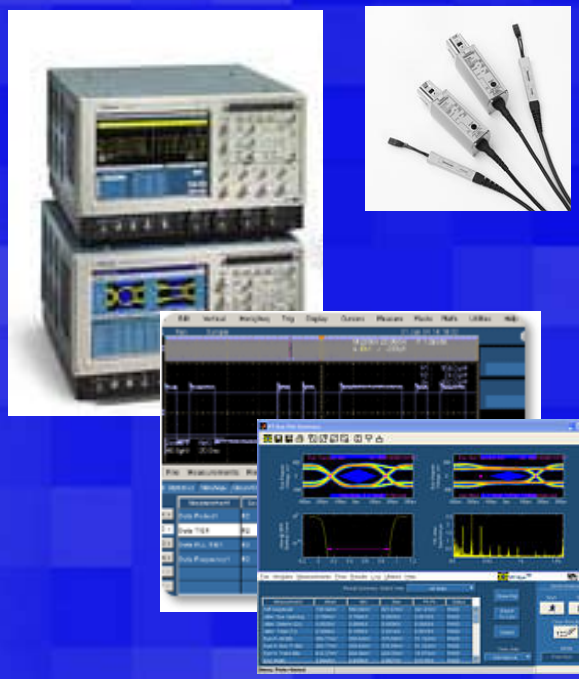
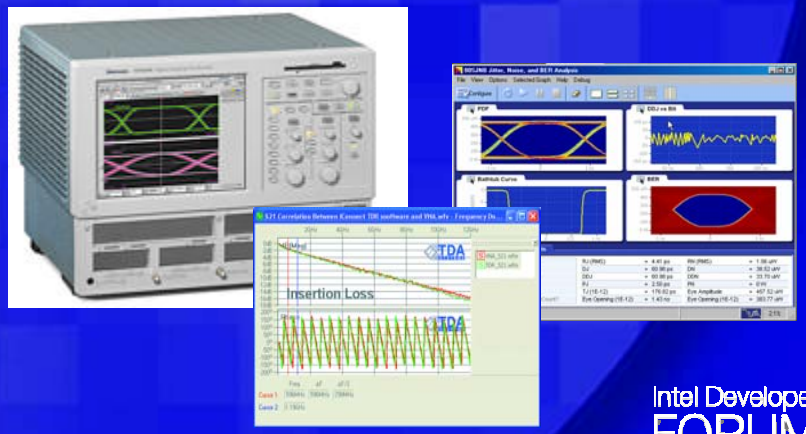
Analog Test Tools for Gen2 Serial

- **Real Time Oscilloscopes**
  - Spec requires >10GHz
  - >12 GHz for 5th Harmonic
    - Accurate to 30ps transition spec
  - >12GHz probing for validation and debug
  - Software for eye & jitter compliance measurements
- **Sampling Oscilloscopes**
  - 70+ Gigahertz
  - Software for S parameter extraction (TDNA)
  - Software for Jitter & Noise at BER





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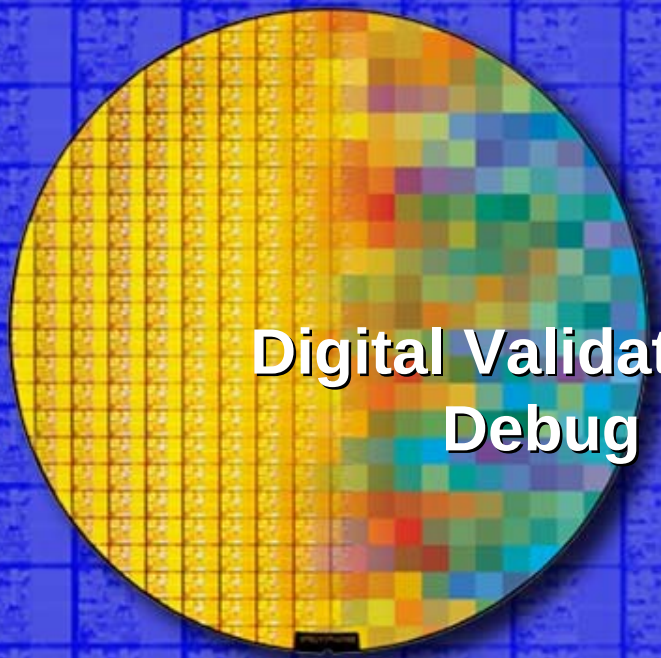
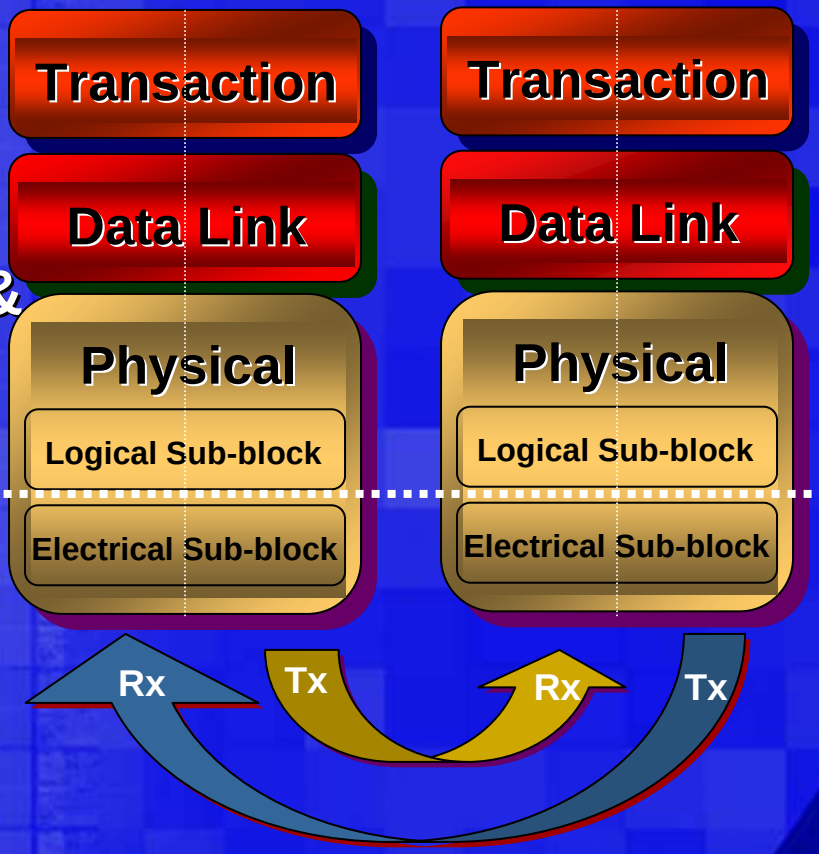
Digital Validation & Debug



Analog Validation &
Compliance



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Gen 2 Design Considerations

- Design for Validation
  - Obtain a copy of the logic analyzer probe design guide requirements
  - Adhere to probe keep out volume requirements
  - Ensure electrical compliance to the PCI Express* specification
- Follow with electrical simulations and keep out volume analysis

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Ensure Electrical Spec Compliance

- Designers must ensure electrical compliance to guarantee system visibility
- Problems encountered during digital validation may be caused by analog characteristics
- Examples
  - Data eye size
  - Jitter
  - Reference clock

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PCI Express* Gen 2 Validation

- Probing
- Acquisition
- Analysis

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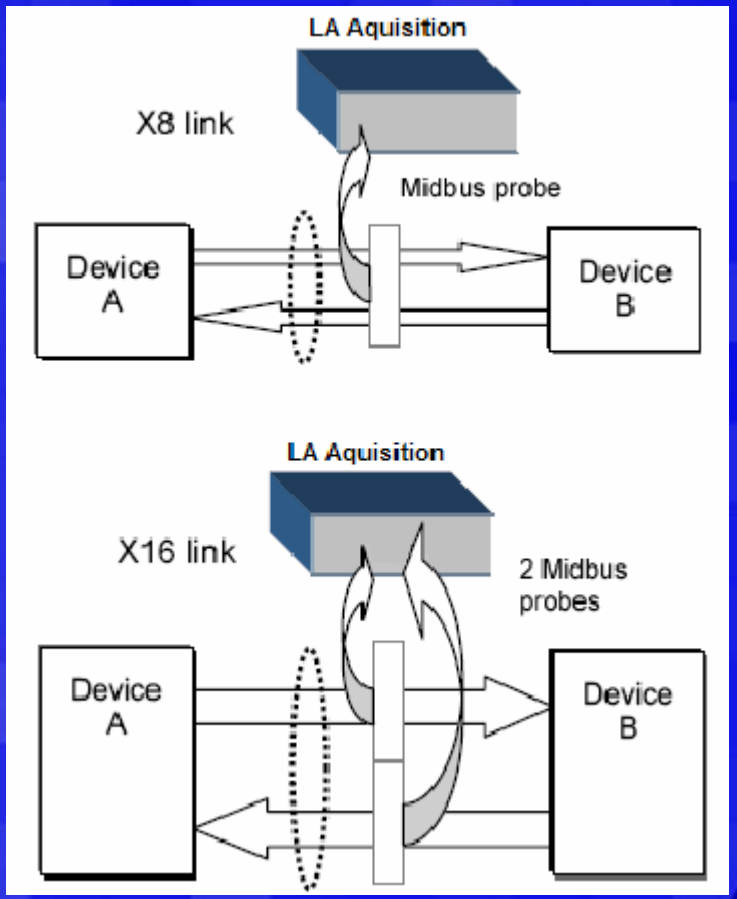
PCI Express* Probe Points

- **Serial Data Probe Points**
  - **Mid-bus**
    - Probe chip to chip links
    - x8 and x16 footprints
  - **Slot Interposer[1]**
    - Probe PCI Express slots
    - x1, x4, x8, x16
  - **Solder down**
    - Probe serial lanes that are physically together



[1] Data shows that a Gen 2 interposer may not be feasible

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Probe Strategy Considerations

- Three probing options

	PROS	CONS
Mid-bus	•Minimum load •Minimum loss	•Requires board space •Must be designed in
Interposer (Data shows that a Gen 2 interposer may not be feasible)	•Does not require board space •Does not have to be designed in	•Extra bus loading •Adds jitter
Solder Down	•Minimum load •Minimum loss •Does not require board space	•Requires two solder connections per lane •Not easily moved from one platform to another

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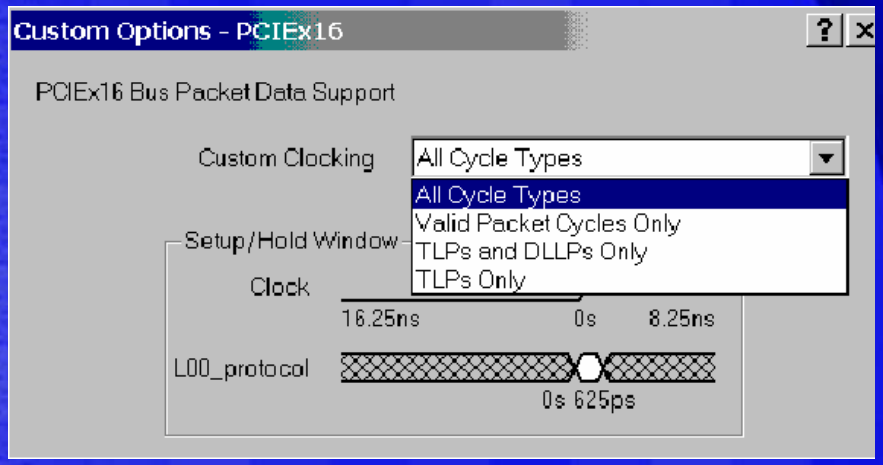
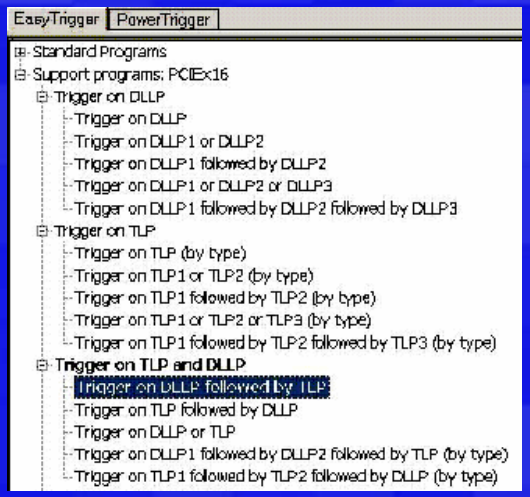
Acquisition

- Capture
  - Acquire Gen 1 and Gen 2 PCI Express data rates
  - Clock qualified filtering
  - Storage qualified filtering



- Triggering
  - Optimized for serial data
  - Capture related Tx and Rx events with cross triggering
  - Predefined trigger programs for triggering on event sequences, packet types, and packet combinations



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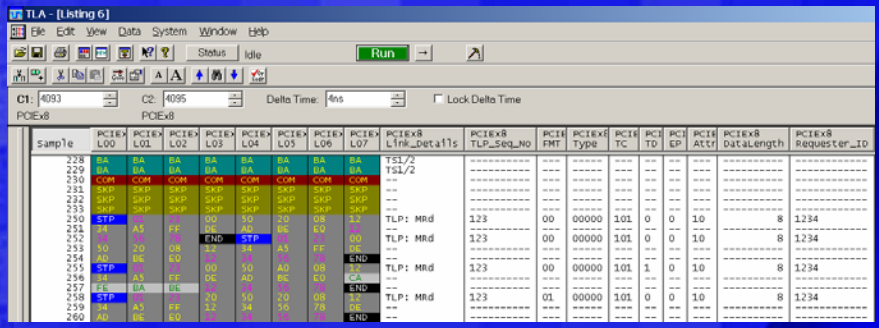
Protocol Decode and Visibility

- Display decoded PCI Express packets
- View disassembled packets within a single transaction across multiple links
- Time correlate data between PCI Express* and other serial or parallel links links via timestamp generator



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Digital Test Tools for Gen 2 PCI Express*

- Logic Analyzers
  - Acquisition of 5Gb/s
    - Overhead suitable for margin testing
  - Mid-bus and interposer[1] probe options
  - Protocol decode software
  - Triggering optimized for serial protocols
  - Cross bus correlation for complete system validation
  - Analog and digital correlation for validating elusive signal integrity problems

[1] Data shows that a Gen 2 interposer may not be feasible

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Summary

- Jitter measurement methods are converging on industry accepted methods of Tj and Dj determination
- Gen-II measurements are a separate class of measurements to those found in Gen-I, however Gen-II compliance requires compliance to both Gen-I and Gen-II requirements
- Knowledge of channel characteristics is key for obtaining effective Gen-II measurements
- Mid-bus logic analyzer probing is recommended for Gen-II
- Adherence to Gen-II electrical specifications is critical for successful digital validation

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Question and Answers

Please fill out the Session Evaluation Form.

Thank You!